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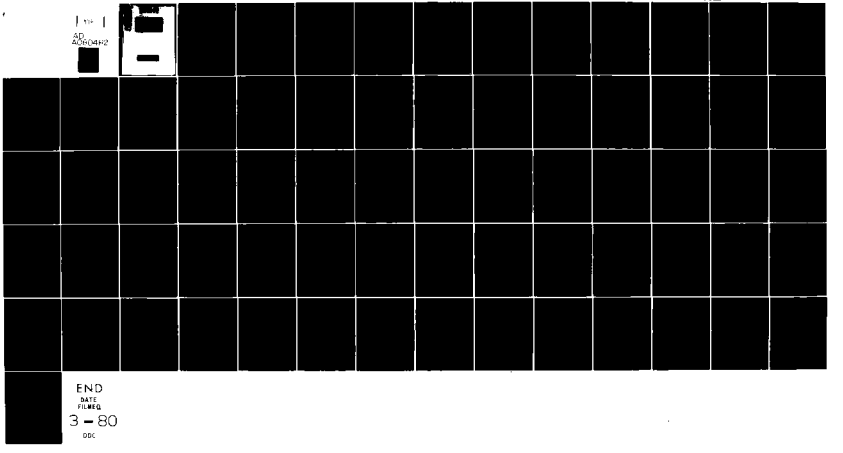

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SOLID STATE POWER CONTROLLERS (ISEM-2A)

P. J. Coyle
C. L. Whitman

Government Communications Systems
Government Systems Division
RCA CORPORATION
Camden, New Jersey 08012

30 November 1979

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proved By: C. T. Shelton
C. T. Shelton, Manager
Communications Equipment

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20. ABSTRACT

This report covers an engineering study to determine the optimum DC power controller configuration for ISEM-2A modules. The study indicates that two 10 amp. or four 5 amp. controllers can be mounted on one ISEM-2A frame, and that each 10 amp. unit will have a predicted reliability of nearly one million hours before failure. Mounting of DC controllers using existing technology is discussed, and thermal performance of various frame material is tabulated and evaluations made. Finally, methods of circuit simplification using recently developed components, LSI and advanced packaging techniques which reduce cost, increase reliability and improve manufacturability are described.

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SUMMARY

This report covers an engineering study to determine the optimum configuration of previously developed electrical designs of 28 volt DC power controllers into the physical and thermal constraints of modular avionics packaging (MAP) concepts. The study indicates that two 10 amp. or four 5 amp. controllers can be mounted on one ISEM-2A frame by using advanced packaging concepts and recently developed components. Furthermore, the reliability prediction for 10 amp. units indicates one million hours before failure by using these techniques. One 10 amp. DC controller using existing hybrids mounted on an ISEM-2A frame is described. Thermal performance of various frame materials is tabulated and evaluations made. Also described are methods of circuit simplification using recently developed components and advanced packaging techniques.

1.0 INTRODUCTION

This study was conducted as a preliminary investigation to determine the feasibility of packaging solid state DC controllers on ISEM-2A boards. The intial approach was to package the existing controller design, which consists of three hybrid boards, making only minor orientation changes. This design allowed only one controller per ISEM-2A frame. Advanced concepts for packaging were developed to increase board populations and to improve manufacturability. Different frame and circuit board materials were evaluated for both packaging schemes from the standpoint of thermal dissipation, structural integrity, manufacturability, weight and cost.

The basic module material combinations investigated were:

1. Alumina on Aluminum
2. BeO on "
3. Alumina on Copper
4. BeO on "
5. Alumina on Copper Clad Aluminum
6. Porcelain on Copper Clad Steel

Alumina on Aluminum (consisting of Alumina substrates, soldered to aluminum frames) was the combination selected for the optimum module design, because of its good heat dissipation, low weight and economy of fabrication.

2.0 PACKAGING EXISTING TECHNOLOGY

2.1 Configuration

The existing solid state DC controller is comprised of three hybrid circuit boards arranged in a "stack" with a hermetic seal over the entire module, as shown in Figure 2-0. To enable packaging of the controller onto an ISEM-2A frame, the circuits were arbitrarily re-configured on an equal circuit area basis to accommodate interconnection in a single plane (as opposed to the vertical stack geometry). The three circuits (Power Switch, Logic/Input/Regulator & Sense Amp/Detector) were positioned and oriented to achieve good thermal performance by locating the power switch (the predominant source of heat) in close proximity to the heat dissipating rib and orienting the power switch so that the four power transistors have their own individual parallel thermal paths by which they conduct their heat to the thermal sink. Conduction was considered the only allowable mode by which heat could be removed from the components.

The input circuit is isolated from the logic circuit by means of three opto-couplers, which are quite bulky in size. Due to the excessive height of the DIP, which houses the opto-coupler, a hole must be punched in the frame and the opto-coupler must be mounted inverted in this hole, on a .030 in. slab of Alumina (see Fig. 2-1 and 2-2). This problem constrained the placement of controllers on each side of a "T" frame. Although there appears to be sufficient room to accommodate two sets of opto-couplers, the cut-outs required

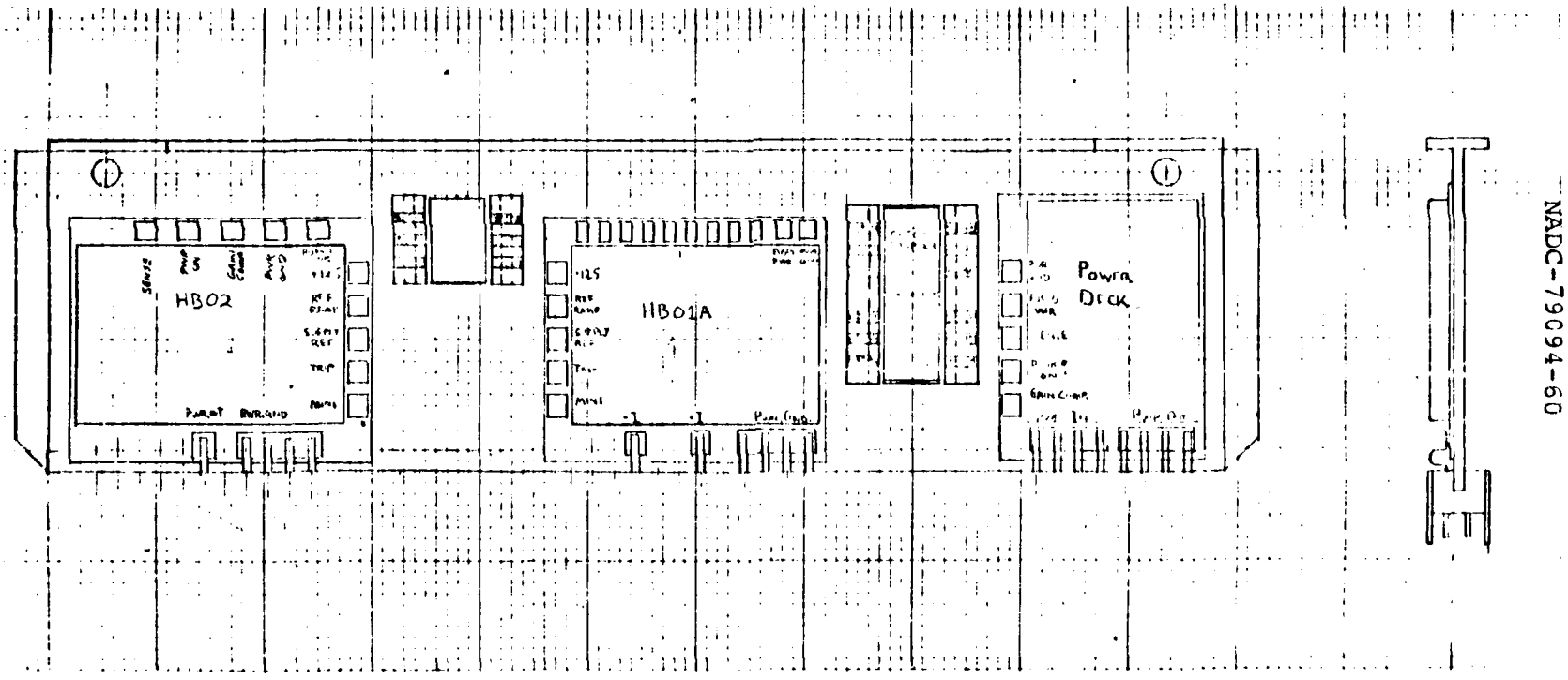

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FIGURE 2-1. MOUNTING EXISTING TECHNOLOGY ON "T" FRAME.

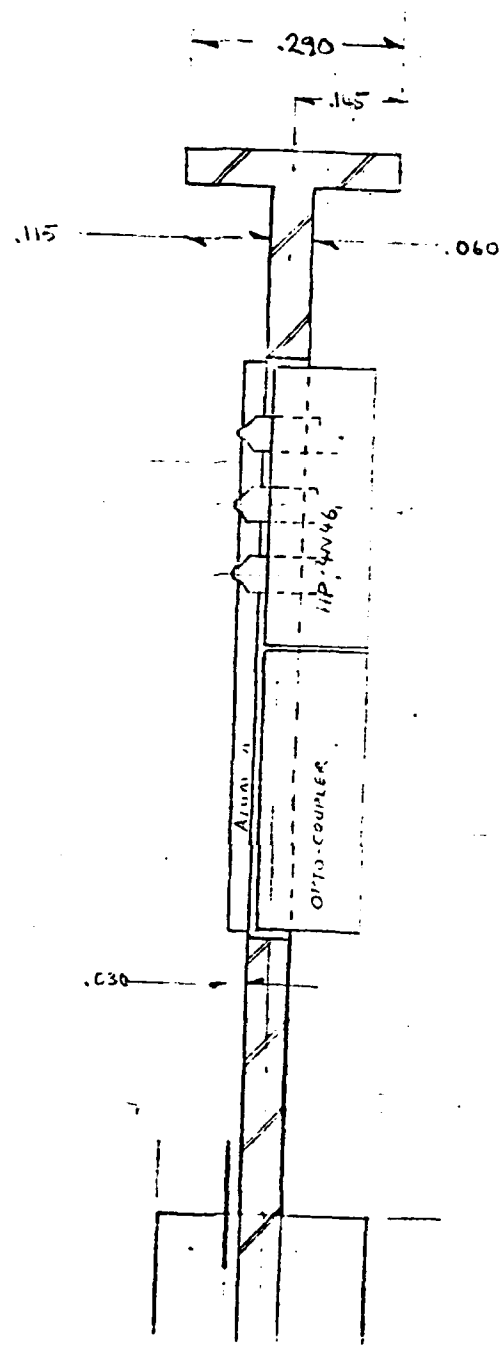

FIGURE 2-2. DETAIL OF OPTO - COUPLER MOUNTING ON "T" FRAME.

would compromise the structural integrity of the module. Even mounting one set of opto-couplers required 2 separate hole locations for this same reason. This limited the population to one controller per ISEM-2A.

Because the control circuitry (Logic/Input/Regulator/Sense Amp/Detector/Opto-Couplers) is the same regardless of the rating of the power switch, only one controller per module is possible. Therefore, there is no advantage to employing a "T" frame because only one side of the frame can be utilized. For this reason, the same circuit was re-configured on a one-sided offset frame. (Ref. NESC Dwg. No. 0102-710). This removed the necessity to punch a hole in the frame to accommodate opto-coupler mounting and allowed the three opto-couplers to be mounted in-line. (See Fig. 2-3). Due to the constraint of packaging only one controller per module, and the fact that the power supply occupies a very small area, integral power supplies for each controller were adopted over a common power supply approach for reliability reasons.

All three hybrid circuit boards contain active components and, therefore, are hermetically sealed with drawn aluminum covers which are soldered to the finished assemblies.

The individual hybrid circuits are then soldered to the metal frame with a low melting point ($\sim$140°C) Indium solder. At the same time, the external electrical connections are made by fluxless reflow soldering the required pins directly to the appropriate pads on the bottom edge of the hybrid substrate.

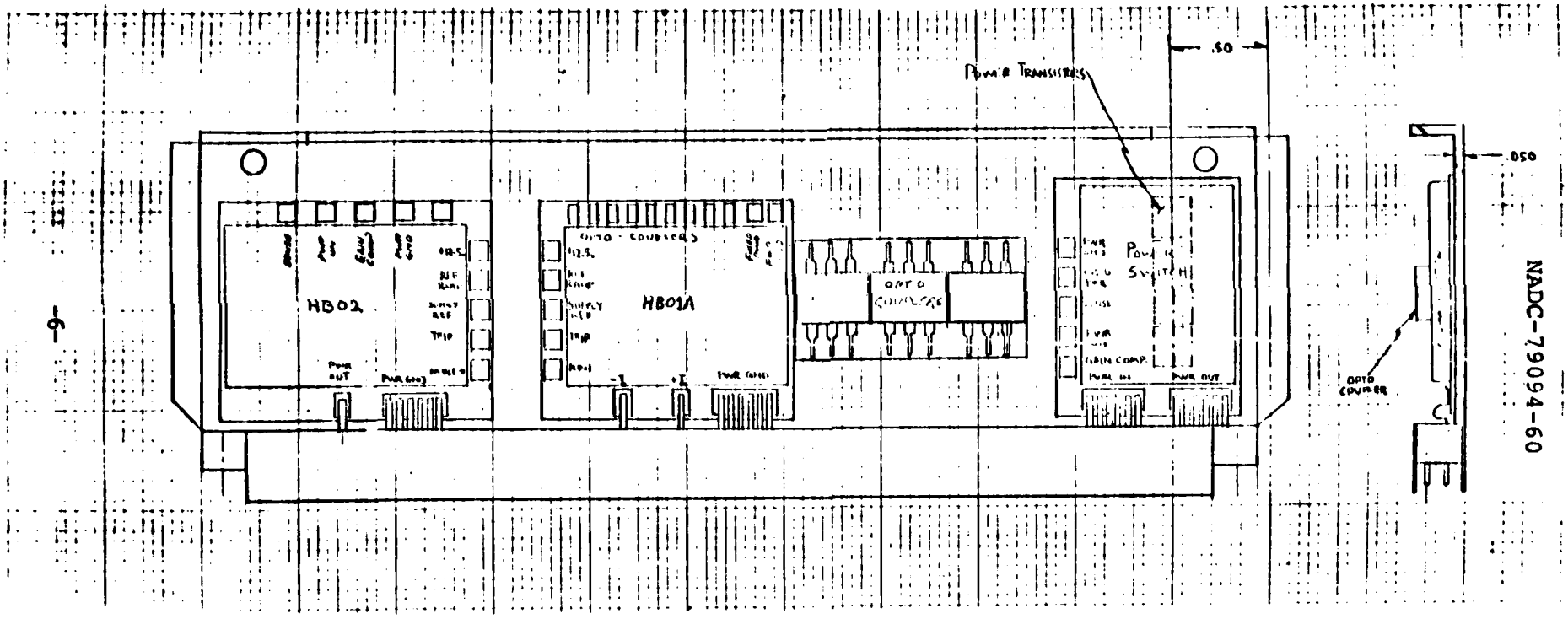

FIGURE 2-3. MOUNTING TECHNOLOGY ON OFF-SET FRAME.

Multiple pins are used for circuits through which there are high current flows (POWER IN & OUT, POWER GROUND) for increased reliability.

2.2 Thermal Design

Eight frame designs were evaluated for their relative thermal dissipation characteristics. Each frame/circuit substrate configuration was evaluated for its ability to transfer heat from the four power transistors used in the 10 amp controller. It is assumed that conduction is the only mode available to transfer heat from the circuit. The thermal performance, therefore, is merely the comparison of the thermal resistance through a path which begins at the device/substrate interface and terminates at the module frame/heat sink interface. The heat dissipated by the transistors, first flows perpendicularly through the electrically insulating substrate, through the bonding material into the thermally conducting frame, then along the frame to the rib which is in contact with the heat sink in the rack structure. The perpendicular thermal resistance is calculated as three resistances in series as follows:

$$\theta_p = \frac{R_1 t_1 + R_2 t_2 + R_3 t_3}{A}$$

where:

θ_p = perpendicular thermal resistance ($^{\circ}C/W$)

R = thermal resistivity ($^{\circ}C$-in/W)

t = thickness of material (in.)

A = effective cross sectional area of thermal path (in^2)

subscripts 1,2,3,...denote materials in flow sequence.

The longitudinal thermal resistance, along the module frame, is calculated by summing the three parallel resistance paths of the substrate, bonding material, if any, and frame, as follows:

$$e_L = \frac{1}{\frac{1}{R_1 L/a_1} + \frac{1}{R_2 L/a_2} + \frac{1}{R_2 L/a_2}}$$

where: e_L = longitudinal thermal resistance ($^oC/W$)

R = thermal resistivity (^oC-in/W)

L = length of thermal path

a = cross sectional area of thermal path (in^2)

$a = t \times W$

t = thickness of material (in)

W = width of thermal path (in)

The thermal performance predicted by this analysis is conservative in that heat spreading along the thermal path was neglected.

Tables 2-1 and 2-2 show the material configurations of the eight module designs and the values used in the calculations, as well as the results. The total resistance of the thermal path is the sum of the perpendicular and longitudinal resistances. The value of the total thermal resistance is the temperature gradient (ΔT) that will exist between the thermal source and the thermal sink per watt to be dissipated. The thermal sink temperature is assumed to equal the outlet air temperature of 70^oC which would be the highest temperature of any thermal

TABLE 2-1. PERPENDICULAR THERMAL RESISTANCE

DESIGN	A	B	C	D	E	F	G	H
MAT'L 1	ALUMINIA	BeO	ALUMINIA	PORCELAIN	ALUMINIA	PORCELAIN	PORCELAIN	ALUMINIA
R_1	2.13	.17	2.13	34.5	2.13	34.5	2.13	34.5
t_1	.025	.025	.025	.006	.025	.006	.025	.006
θ_1	.33	.03	.33	1.29	.33	1.29	.33	1.29
MAT'L 2	SOLDER	SOLDER	SOLDER	COPPER	SOLDER	COPPER	SOLDER	COPPER
R_2	.76	.76	.76	.11	.76	.11	.76	.11
t_2	.004	.004	.004	.005	.004	.010	.004	.020
θ_2	.02	.02	.02	.003	.02	.006	.02	.012
MAT'L 3	ALUMINUM	ALUMINUM	ALUMINUM	STEEL	COPPER	STEEL	COPPER	STEEL
R_3	.23	.23	.23	.85	.11	.85	.11	.85
t_3	.050	.050	.030	.050	.02	.040	.050	.050
θ_3	.07	.07	.04	.27	.012	.21	.03	.27
MAT'L 4					STEEL			
R_4					.85			
t_4					.030			
θ_4					.16			
θ_p =	.42	.12	.39	1.56	0.52	1.51	.38	1.57

TABLE 2.2 LONGITUDINAL THERMAL RESISTANCE

DESIGN	A	B	C	D	E	F	G	H
Mat'l. 1	Alumina	BeO	Alumina	Porcelain	Alumina	Porcelain	Porcelain	Alumina
R_1 (°C in/W)	2.13	.17	2.13	34.5	2.13	34.5	34.5	2.13
t_1 (in)	.025	.025	.025	.006	.025	.006	.006	.025
A_1(in²)(1 in X W_1)	.025	.025	.025	.006	.025	.006	.006	.025
Mat'l. 2	Solder	Solder	Solder	Copper	Solder	Copper	Cu	Solder
R_2	0.76	0.76	0.76	.11	.76	.11	.11	.76
t_2	0.004	0.004	0.004	.005	.004	.010*	.020**	.004
A_2(1 in X W_2)	0.004	0.004	0.004	.005	.004	.010	.020	.004
Mat'l. 3	Aluminum	Aluminum	Aluminum	Steel	Cu	Steel	Steel	Copper
R_3	0.23	0.23	0.23	0.85	.11	0.85	.85	0.11
t_3	0.050	0.050	0.03	0.050	.02**	0.040	.050	.050
A_3(1 in X W_3)	0.050	0.050	0.03	0.050	.02	0.040	.050	.050
Mat'l. 4					Steel			
R_4					.85			
t_4					.030			
A_4					.030			
Θ_L (°C/w)	2.13	1.35	3.40	4.78	2.14	3.61	2.07	1.06
Θ_p	.42	.12	.39	1.56	.52	1.51	1.57	.38
Θ_{RT}	2.55	1.47	3.79	6.34	2.66	5.12	3.64	1.44
ΔT (ol)	38°C	22°C	57°C	95°C	40°C	77°C	55°C	22°C
Wt. (lb/in²)	0.011	0.010	0.0076	0.016	0.020	0.015	.021	.021
T_{device} @T_{sink}=70°C	138	122	157°C	195°C	140°C	177°C	155°C	122°C

* .005 in of Cu is deposited on each side
** .010 in of Cu is deposited on each side

sink in the rack.[1] The predicted device temperature is calculated as follows:

$$T_D = \Delta T + T_{sink} + e_c q$$

$$\Delta T = e_{TOT} q$$

where: T_D = device temperature (^oC)

e_{TOT} = $e_P + e_L$ total thermal path resistance ($^oC/W$)

e_c = Rib/sink interface contact resistance ($^oC/W$) = 2 $^oC/W$

q = power dissipation (Watts) = 15W

T_{sink} = temperature of thermal sink (^oC) = 70^oC

Module designs A,B,C consist of Alumina or BeO substrates soldered to aluminum frames. Module designs D,E,F,G consist of porcelain on copper clad steel frames. (Module design H consists of alumina substrate soldered to a solid copper frame).

The last item of importance listed in the table, is the module weight per square inch of frame area. This figure includes the substrate, bonding material, if any, and frame weight. The component weights are not included, since they are common to all designs.

A frame thickness of .050 in. is desirable to minimize the

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1 Ref. - JTIDS Partitioning Study, (final report) Data Item A002 Prepared for NADC by Singer-Kearfott Div.

required machining operations as this is the guide rib thickness. Aluminum frames, whether standard "T" or off-set configuration, can be made from an extrusion. The cost of extruded material is the amortized cost of the extrusion die, plus the cost of the aluminum, on a weight basis, which is constant, regardless of the intricacy of the extruded part. The off-set frame design would require a stamping operation to form the guide ribs into the proper location. Both designs would require machining the extractor holes and related clearances, in the top rib for the extractor tool.

Porcelain on steel boards, which are considered to be low cost substrate/frame assemblies, cannot be extruded into intricate shapes and, therefore, rely on more expensive machining operations. The top rib can be formed in a bending operation for the offset frame design. However, for the standard "T" frame design, a separate piece must be fabricated and attached to the steel frame. These additional fabrication costs may be offset by the savings realized by omitting the substrate to frame assembly step which is required with aluminum frame. Due to the poor thermal performance of standard porcelain on steel, porcelain on copper clad steel was pursued as an improved structure. This, however, will increase the cost of the frame.

There are two schemes by which the DC controller could be attached to the porcelain on copper clad steel frame:

1) The existing hybrid circuitry could be fabricated using the

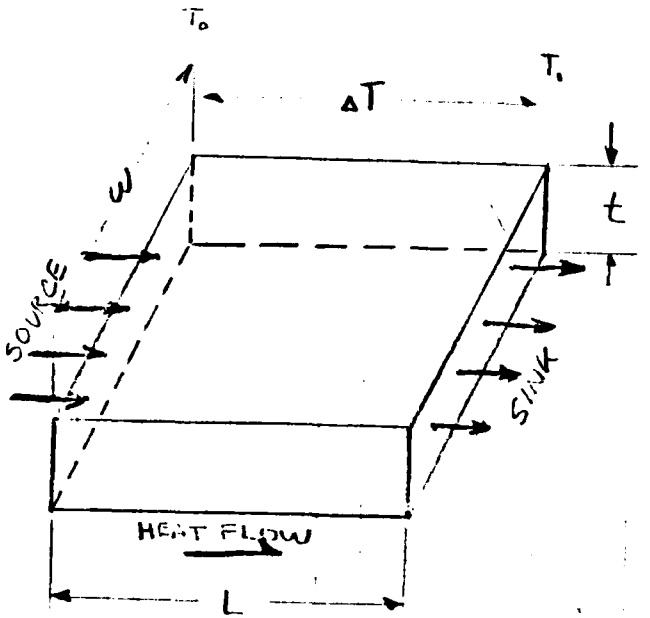
porcelain as a substrate. (Design D & F). All necessary interconnection of the various circuits could then be accomplished by thick film conductors. This method of interconnection has the potential of reducing production costs. However, this is an immature technology.

2) The circuits could be fabricated on alumina and/or beryllia oxide substrates. The porcelain would be removed from the appropriate areas on the frame and the copper metallized bottoms of the substrates would be soldered to the copper clad steel directly. Frame Design (E) uses this construction and attained the best thermal performance of any of the steel frames investigated. The interconnection could then be by thick film conductors which had been previously fired onto the porcelain surface. The hybrid circuits would then be bridged to the interco nection network by reflow soldering the tabs at the same time the substrate is soldered to the frame.

Only one of the porcelain designs (G) is marginally acceptable from a thermal standpoint and this design requires cladding the steel with 10 mils of copper on each side of a 50 mil steel core. This frame weighs more than twice as much as an alumina/aluminum frame of equivalent thermal performance (C). For these reasons, porcelain on steel has been eliminated from consideration. The modified porcelain on steel design (E)

performed well thermally but cost and weight are prohibitive. Although the copper frame (H) is the best thermal performer, it is as heavy as the previously mentioned frame design (G). The copper frame could be thinner and, therefore, lighter and still have adequate thermal performance but would be structurally inadequate. The copper frame would also cost almost 4.5 times that of the aluminum. Frame (B) is of equivalent thermal performance of frame design (G). This is accomplished by substituting beryllia oxide (BeO) for the alumina substrate. Beryllia oxide is expensive and special precautions must be observed when machining it, and is, therefore, undesirable. Frame design (A), which uses an alumina substrate, adequately satisfies the thermal requirements and is almost half the weight of the copper frame design (H) or steel frame design (E) or (G).

For any given configuration, for a conductive heat exchanger, aluminum can conduct a unit of heat with the least amount of mass. Consider the three candidate materials: aluminum, copper and steel. Now, consider a segment of the frame which is one inch wide and one inch long of thickness. Heat is to be conducted along the length of the frame segment from source to sink. (See Fig. 2-4). For a gradient of 10°C and a thickness of 0.1 in a segment made of aluminum can transfer 4.35 watts of heat, as shown in Table 2-3. Under the same conditions, a segment of copper would only have to be 0.048 in. thk. and a segment of steel would have to be .370 in. thick to transfer



$\Delta T = 10^{\circ}C$

$L = 1.0$ IN.

$W = 1.0$ IN.

FIGURE 2-4. HEAT TRANSMISSION MODEL.

TABLE 2-3. WEIGHT AND RELATIVE COST OF ALUMINUM, COPPER AND STEEL FRAMES

	K(W/IN °C)	t(in.)	VOLUME (in^3)	(lbm/in^3)	WT. (lbm)	RELATIVE WT.	COST $/lbm	EFFECTIVE COST	RELATIVE COST
ALUMINUM	4.35	0.10	0.10	.098	.0098	1.0	0.66	.0065	1.0
COPPER	9.10	0.048	0.048	.323	.0155	1.58	0.90	.0140	2.15
STEEL	1.18	0.370	0.370	.283	.105	10.71	0.20	.0210	3.23

ℓ = thickness of material required to conduct 4.35 watts

Effective Cost = (wt. of frame segment) x (Cost/lbm)

This gives a ranking of material cost per unit of heat it can transfer.

the same quantity of heat. The weight of the segments are the products of the material volumes (W x L xt) and densities (p) which are .0098 lb for aluminum, .0155 lb. for copper and 0.105 lb. for steel. Therefore, a steel heat exchanger would have to weigh more than ten times that of a aluminum heat exchanger of equal thermal capacity. A copper heat exchanger would weigh 58% more than an aluminum one, however, the frame would be less than half the thickness which would be an important advantage if additional circuit height was needed. Therefore, in avionics modules requiring high rates of heat dissipation, aluminum is the most desirable material.

Table 2-3 also relates the relative costs of the three frame materials. The effective cost is the product of the material weight of the frame segment and the cost per pound. This provides a relative ranking of the cost of the material per unit of heat it can transfer. Aluminum, as well as being the most weight effective, is also the most cost effective. A copper heat exchanger of equal conductive capacity would cost more than twice as much and an equivalent steel heat exchanger would cost more than three times as much.

3.0 ADVANCED PACKAGING CONCEPTS

3.1 Electrical Design Considerations

Recent developments in the power FET art, have brought forth a new line of devices, with many favorable characteristics, especially suited for power switches. Among these desirable features are:

- o low driving power.
- o low saturation resistance.
- o high input impedence.
- o better adaptation to paralleling.

A device with particularly favorable characteristics for power switching is shown in Appendix A.

Since the power MOSFET is responsive to voltage at very low gate current, low quiescent power drain can be achieved without the need for regenerative drive to provide overload output capability. Hence, the driving circuitry of the existing controller design, shown in Figure 3-1, can be considerably simplified. Referring to Figure 3-1, driver transistors Q8, Q10, Q12 and Q14 will not be needed with MOSFET devices, and regenerative amplifier transistors Q3 and Q5 will also be eliminated. The amplifier hybrid, shown in Figure 3-2, will also be affected by the elimination of IC U5/C and U6/D.

The high input impedance of the MOSFET can be used to good advantage in the simplification of circuitry required for

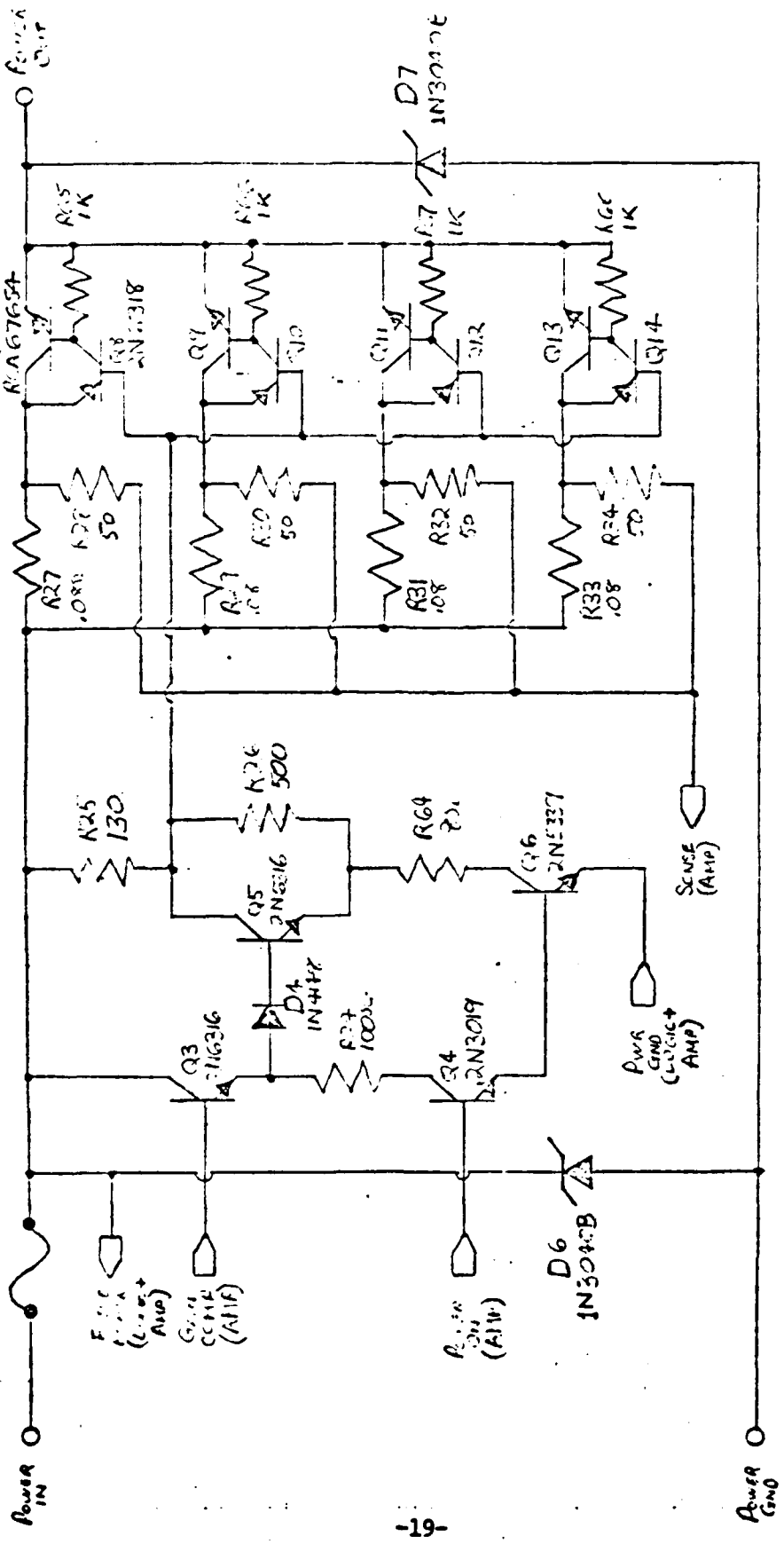


FIGURE 3-1. SCHEMATIC DIAGRAM OF POWER HYBRID (HA01).

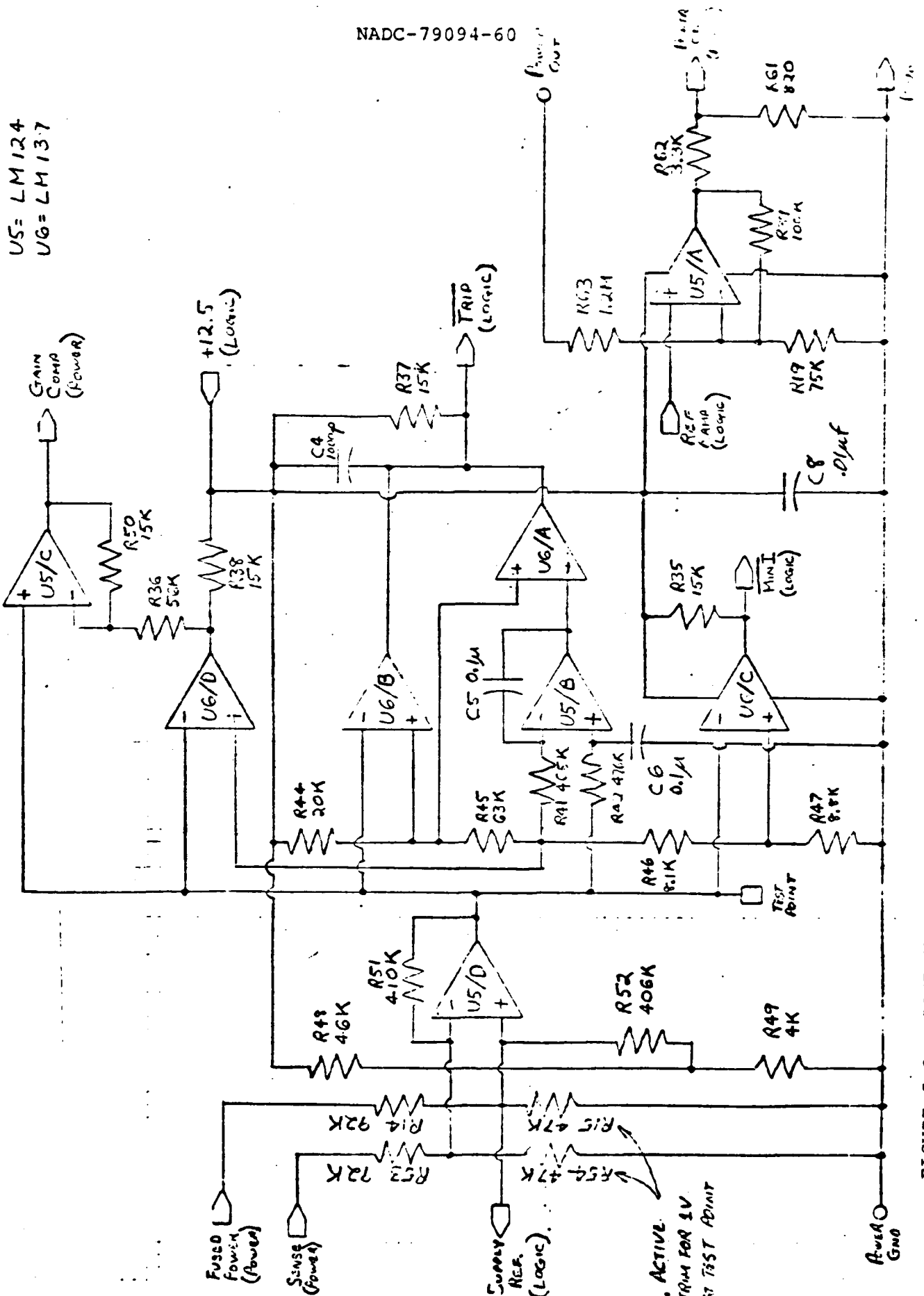


FIGURE 3-2. SCHEMATIC DIAGRAM OF AMPLIFIER HYBRID (IIB02)

output voltage shaping. Simple RC networks can then be used at the gates of the MOSFET devices to provide the desired output rise and fall timing. This circuit simplification will result in the elimination of one operational amplifier, U5/A, and associated resistors in the amplifier hybrid, shown in Figure 3-2, and transistors Q17 and Q18, with associated resistors in the logic hybrid, shown in Figure 3-3.

A schematic diagram of the proposed output switching circuit using two type IRF-150 MOSFET's, is shown in Figure 3-4. Because of the low saturation resistance and high power handling capability of these devices, only two units are used in parallel. The 15 volt, low current power supply is needed to furnish a high positive rate to drain voltage for MOSFET's Q103 and Q104 at 1000% output overload. Transistor Q101 can be driven directly from the logic circuitry U2/D, shown in Figure 3-3. Output voltage shaping is provided by the RC network composed of R108, R109 and C101.

The net result of the preceeding design simplifications is the elimination of the following parts:

Transistors	-	10
Diodes	-	2
Resistors	-	27

These advanced design concepts will form a basis for the packaging techniques which follow.

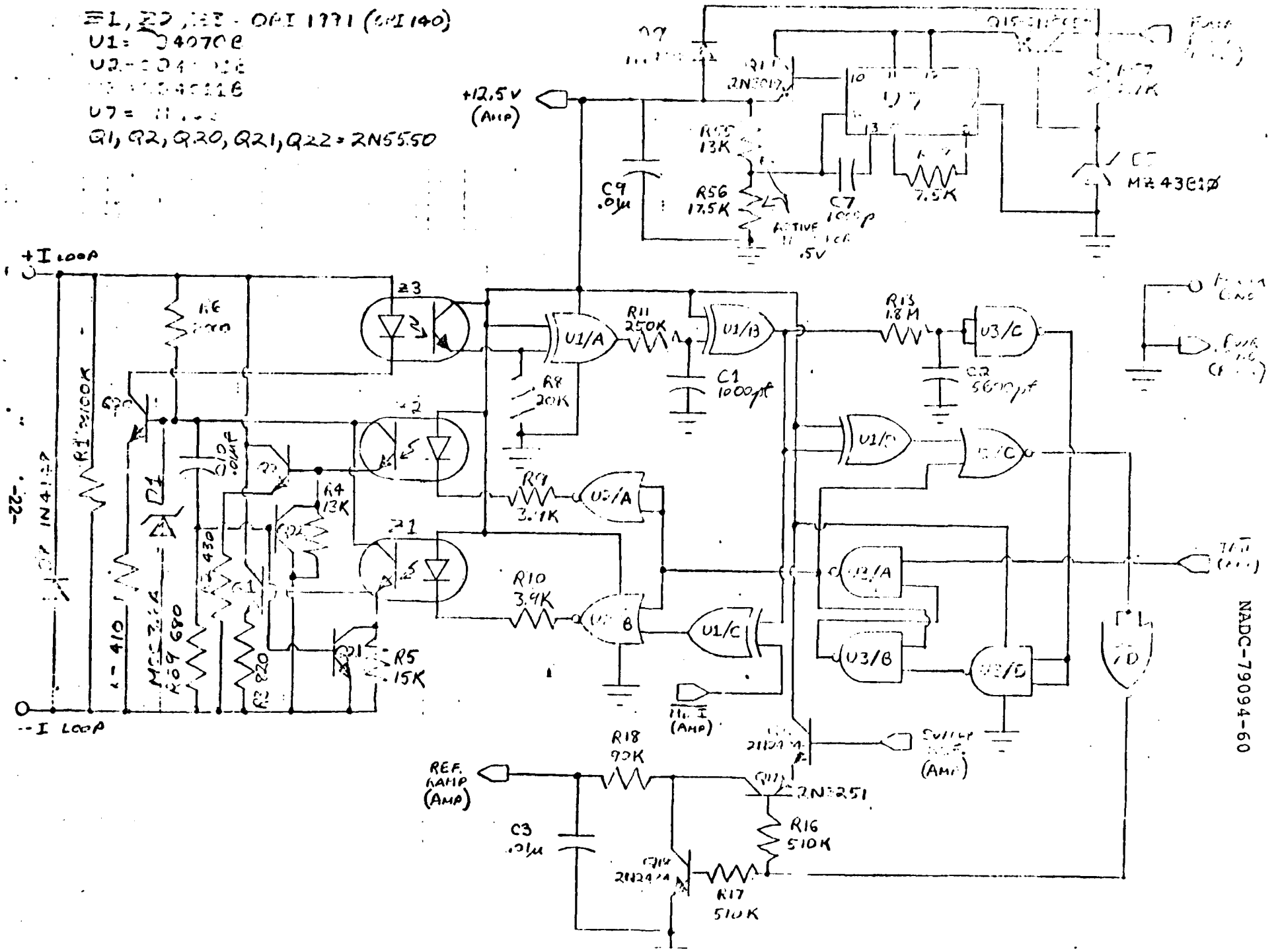


FIGURE 3.3 SCHEMATIC DIAGRAM OF LOGIC/INPUT HYBRID (IHB01)

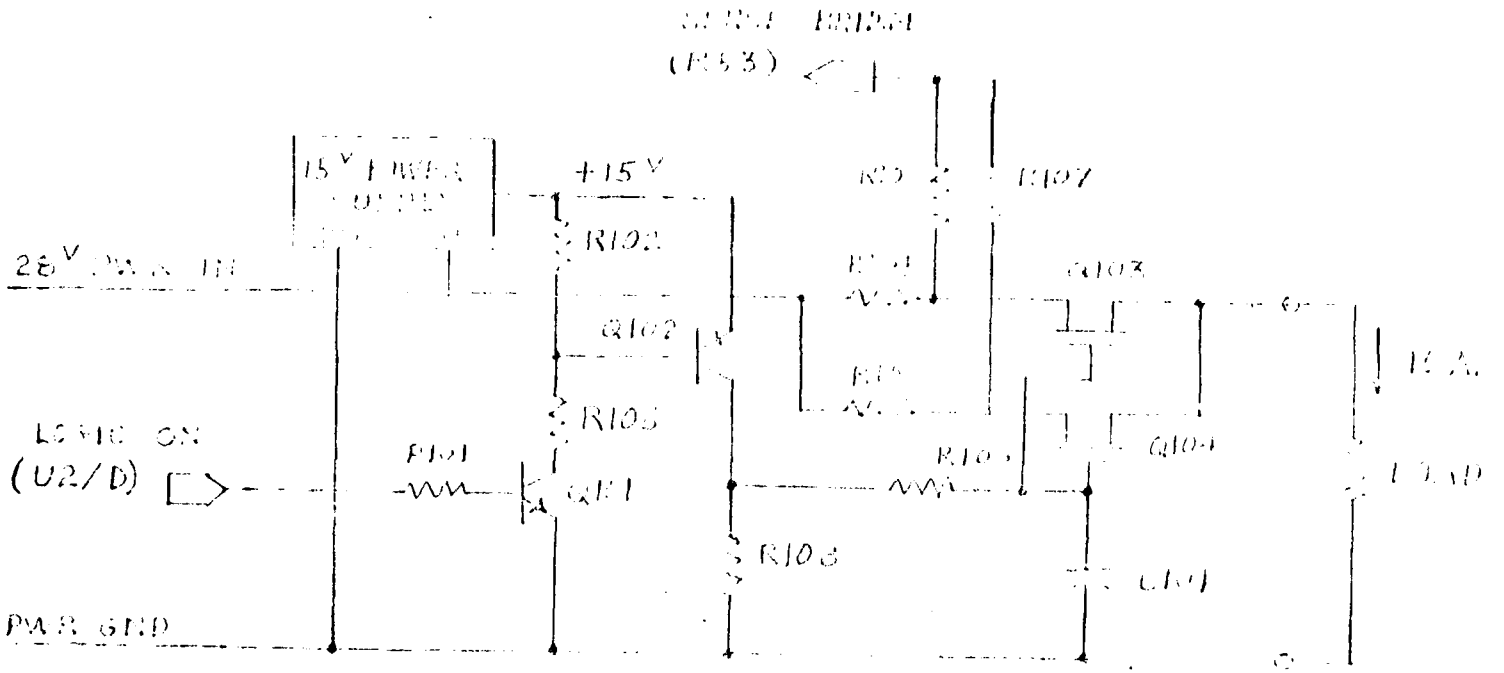


FIGURE 3.4 FUNCTIONAL SCHEMATIC DIAGRAM OF 10 AMP. POWER SWITCH USING HIGH POWER MOSFET DEVICES (Q103 & Q104)

3.2 Advanced Configuration

The one advantage of packaging the existing technology is that it could be implemented in the near term. The disadvantages are numerous. A good deal of room on the module is wasted. Because the circuits are segregated onto three separate substrates, a fair fraction of the module area is dedicated to interconnection pads. The three DIP opto-couplers also consume excessive space on the module. In the three substrate design, the large area of exposed aluminum creates a potential for short circuits to occur. Therefore, all interconnections between the three substrates must be made with insulated wires which then have to be potted to prevent accidental breakage of the wires. The task of reflow soldering the controller to the aluminum frame is also more difficult, since three separate substrates must be attached at once. Due to the numerous active components which are distributed throughout the three circuit boards, each substrate must be hermetically sealed with a drawn aluminum cap. These separate active devices also impose manufacturing problems, in that they are difficult to repair.

In order to improve circuit packing density and manufacturability, advanced packaging concepts were pursued. The control circuitry comprises a large fraction of the controller and is common to all power ratings. Therefore, compacting the control segment is important to achieve higher population density. The circuits can be redesigned, as described in Section 3.1

above, to eliminate some of the components. Also, individual active components, which are distributed throughout the circuit can be combined into an LSI configuration which will greatly reduce circuit area. The logic and the sense amp/detector circuits, can be put on two 175 mil square chips which would then be mounted in a 24 pin leadless chip carrier. (Fig. 3-5). The four power transistors can be replaced with two power FET's of approximately 250 mils square, which would be mounted in two, 32 pin leadless chip carriers. Although the power switch does not occupy excessive room on the existing controller, the chip carrier packaging approach increases manufacturability and repairability.

The opto-coupler portion of the controller had limited the placement of controllers on each side of an ISEM-2A, due to excessive height of the DIP packaging. It is proposed to construct custom opto-couplers inside of an oblong three compartment leadless chip carrier. This would allow two-sided modules, by virtue of the reduced component height. The remaining portion of the controller would be fabricated in hybrid fashion, directly on the same substrate that the leadless chip carriers would be attached to. The voltage regulator and the FET driver stage would be contained under one hermetically sealed cap and the input circuit under another. This packaging method would increase manufacturing yield by allowing the active components to be tested in advance, in their respective chip carriers, before attaching them to the substrate and would also allow easy repair.

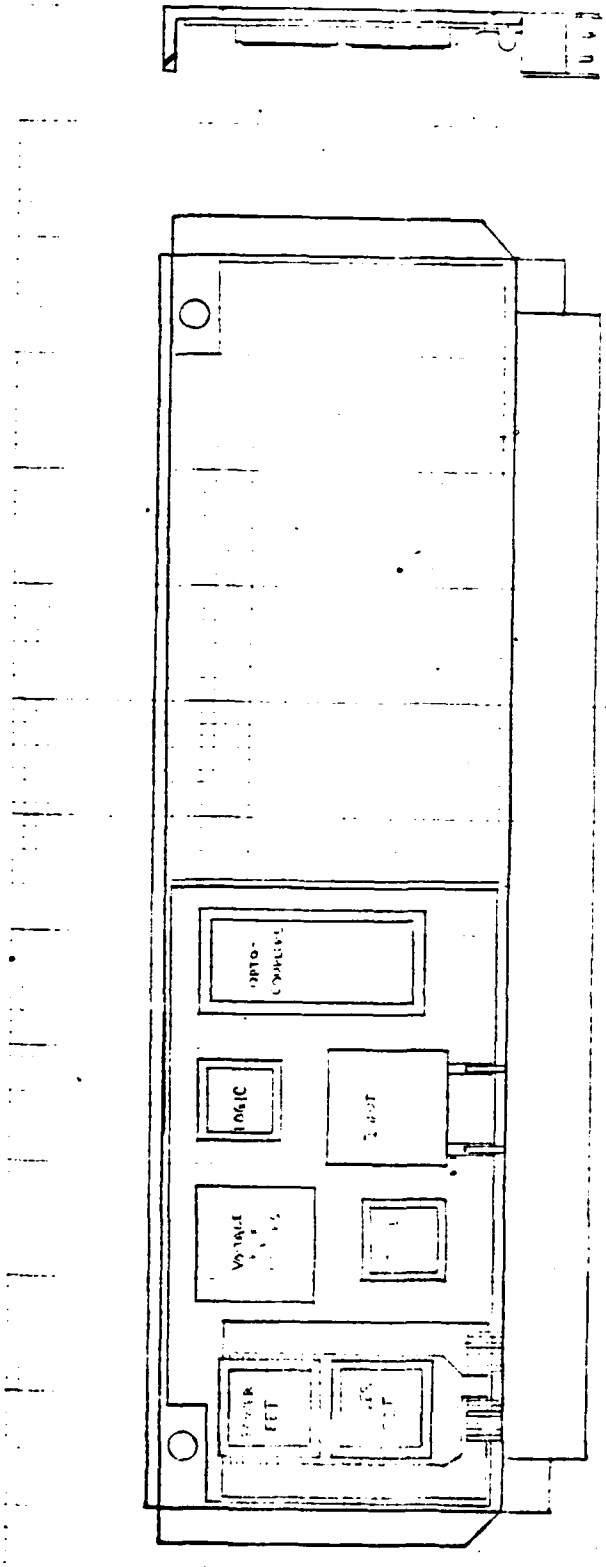


FIGURE 3-5. MOUNTING OF TWO 10-AMP ADVANCED TECHNOLOGY UNITS ON OFF-SET FRAME. SINGLE UNIT SHOWN.

Each controller would have its own substrate. This approach increases yield in manufacturing when compared to multiple controllers occupying a single substrate. All connections to the pin connector are performed at the same time as the substrate is reflow soldered to the frame.

To ensure a voidless solder joint over such a large area (half the frame area) the solder bonding should be carried out as follows:

1. Both copper metallized substrate bottom and appropriate frame area should be solder tinned with approximately 3 mils of solder, each surface. All flux shall then be removed from both surfaces.
2. Assembly should be fixtured to prevent substrate from moving laterally with respect to the frame.
3. Place entire assembly on top of a heat source inside of a Bell jar.
4. Evacuate Bell jar to < 1 torr. absolute pressure.
5. Heat assembly to a temperature which exceeds its melting point by approximately 25%.
6. Maintain heat and break vacuum while solder is in liquid state. Any void in solder joint will collapse yielding a perfect thermal interface.

The overheating is to allow for cool down of the solder by the influx of cool air when the vacuum is released. It is desirable to maintain the solder in a liquid state until atmospheric pressure is attained in the chamber to prevent the

formation of vacuum voids in the solder.

3.3 Thermal Performance

The thermal performance of the advanced packaging design is not as good as the basic design discussed earlier. This is due to two factors. First, the power FET's have a higher power density (i e. W/in^2) which reduces the width of the thermal path. Second, and not as influential, there is an additional thermal impedance in the thermal circuit, that of the chip carrier base. The analysis is even more conservative for these designs (S to Z) than in designs (A to H) because the aspect ratio of the longitudinal path width to length was 1:1 for the former and 2:1 for the latter. The actual heat flow diverges as it proceeds toward the thermal sink. Figure 3-6 depicts a prediction of what the actual heat flow would look like. In addition, use of beryllia oxide chip carriers would also tend to increase the initial spreading of the heat which would, in turn, increase the longitudinal thermal path width. A 3 dimensional multi-mode thermal analysis is required to model this system accurately, but is beyond the scope of this study.

This analysis, however, presents an accurate relative ranking of the various frame/substrate designs. The materials configuration compared in Tables 3-1 and 3-2, are shown in Figure 3-7. Design (W) consisting of a BeO chip carrier and substrate, soldered to a copper frame achieved the best thermal performance with a predicted maximum device temperature of $129^{o}C$. The next best performer was design (V) which substitutes an

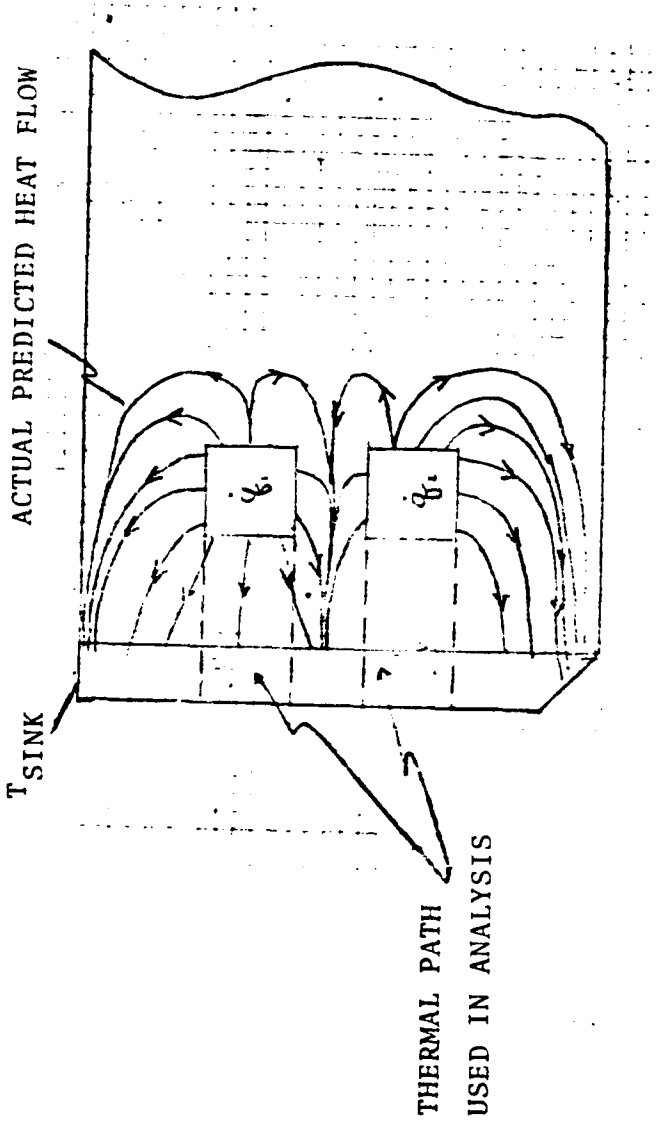


FIGURE 3-6. THERMAL PATH MODEL FOR SIDE-BY-SIDE TRANSISTORS.

TABLE 3-1. PERPENDICULAR THERMAL RESISTANCE (ADVANCED TECHNOLOGY)

DESIGN	T	U	V	W	X	Y	Z	S
MAT'L 1	ALUMINIA	BeO	BeO	BeO	BeO	BeO	BeO	ALUMINIA
R.(OCin/W)	2.13	.17	.17	.17	.17	.17	.17	2.13
t. (in)	.015	.015	.015	.015	.021**	.015	.021**	.040*
θ_{P1} (OC/W)	.51	.04	.04	.04	.06	.04	.06	1.36
MAT'L 2	SOLDER	SOLDER	SOLDER	SOLDER	SOLDER	PORCELAIN	SOLDER	SOLDER
R_2	.76	.76	.76	.76	.76	34.5	.76	.76
t_2	.005*	.005*	.005	.005*	.001	.006	.001	.005
θ_{P2}	.061	.061	.061	.061	.012	3.31	.012	.061
MAT'L 3	ALUMINIA	ALUMINIA	BeO	BeO	CU	CU	CU	CU
R_3	2.13	2.13	0.17	0.17	.11	.11	.11	.11
t_3	.025	.025	.025	.025	.010	.010	.020	.010
θ_{P3}	.85	.85	.07	.07	.02	.02	.04	.02
MAT'L 4	ALUMINUM	ALUMINUM	ALUMINUM	CU	STEEL	STEEL	STEEL	ALUMINUM
R_4	.23	.23	.23	.11	.85	.85	.85	.23
t_4	.05	.05	.05	.05	.04	.04	.07	.04
θ_{P4}	.18	.18	.18	.09	.54	.54	.95	.15
θ_{PTotal}	1.60	1.13	0.35	0.26	.61 (Porcelain Removed)	3.91	1.06 (Porcelain Removed)	1.59

* .004 between substrate and frame + .001 under chip carrier

** Special chip carrier has extender base with deposited Cu to allow soldering the carrier directly to the frame metal by removing the porcelain in the appropriate areas.

TABLE 3-2. LONGITUDINAL THERMAL RESISTANCE (ADVANCED TECHNOLOGY)

DESIGN	T	U	V	W	X	Y	Z	S
MAT'L 1								ALUMINA
$R_1(\frac{(OC\text{-}in)}{W})$								2.13
t_1 (in)								.025
A_1 (in^2)								.0075
MAT'L 2	SOLDER	SOLDER	SOLDER	SOLDER	SOLDER	PORCELAIN	SOLDER	SOLDER
R_2	.76	.76	.76	.76	.76	34.5	.76	.76
t_2	.004	.004	.004	.004	.001	.006	.001	.004
A_2	.002	.002	.002	.002	.001	.006	.001	.002
MAT'L 3	ALUMINA	ALUMINA	Be^O	Be^O	COPPER	COPPER	COPPER	COPPER
R_3	2.13	2.13	.17	.17	.11	.11	.11	.11
t_3	.025	.025	.025	.025	.01	.01	.02	.01
A_3	.0125	.0125	.0125	.0125	.005	.005	.01	.005
MAT'L 4	AL.	AL.	AL.	COPPER	STEEL	STEEL	STEEL	AL.
R_4	.23	.23	.23	.11	.85	.85	.85	.23
t_4	.05	.05	.05	.05	.04	.04	.07	.04
A_4	.025	.025	.025	.025	.020	.020	.035	.02
$\theta_{L\ Tot}$	4.25	4.25	2.70	1.65	7.24	7.24	3.78	3.62
$\theta_{P\ Tot}$	1.60	1.13	0.35	0.26	0.61	3.91	1.06	1.59
θ_{Total}	5.85	5.38	3.05	1.97	7.85	11.15	4.84	5.21
GRADIENT ΔT	88°C	81°C	46°C	29°C	118°C	167°C	73°C	78°C
$WT_{single\ sided}$ (lb/in^2)	0.011	0.011	0.010	0.020	0.015	0.015	0.027	0.012
DEVICE TEMP.	188°C	181°C	146°C	129°C	218°C	267°C	173°C	178°C

Thermal Path Width W = 0.5 in. ~ L (Thermal Path Length)

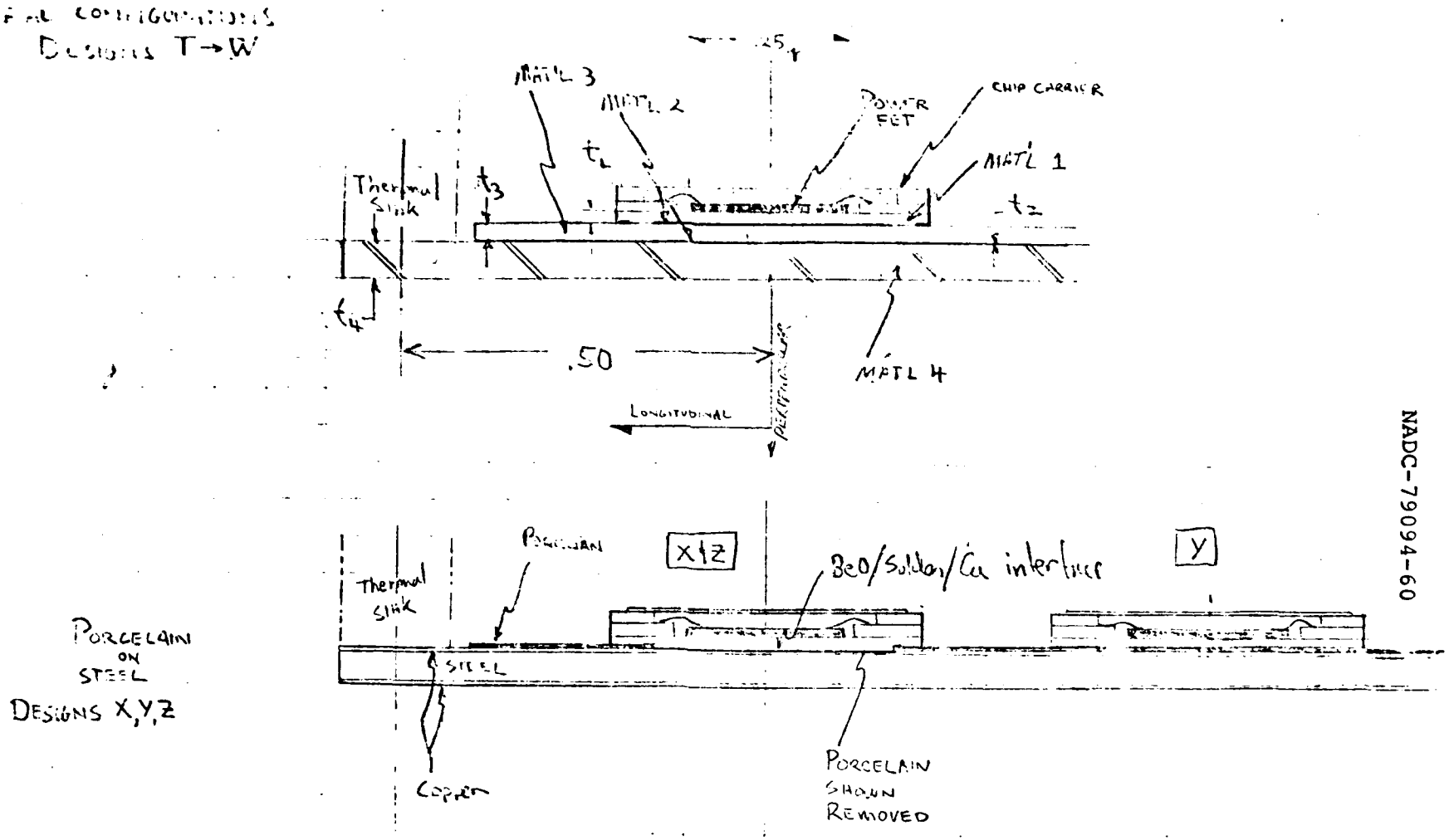


FIGURE 3-7. CONFIGURATION OF CARRIERS FOR POWER TRANSISTORS

aluminum frame for the copper one of design (W). The peak device temperature of 146°C is 13% higher than the copper frame, however, it weighs half the amount. Design (Z), a (70 mil) steel core frame with 10 mils of copper clad to each side with direct solder bonding of the BeO chip carrier onto the copper surface, achieved a predicted peak device temperature of 173°C. Design S, which consists of BeO carrier and alumina substrate soldered to a copper clad aluminum core, ran the device 5°C hotter than Design (Z) but weighed less than half. Design (U), a similar version to (S), without the clad copper, had a device temperature of 181°C, only 3°C higher. The 1.7% gain in thermal performance is hardly worth the additional cost of the clad copper.

Alumina is the best choice for substrate material, due to economy and ease of fabrication. Substrates made of beryllia oxide are even more cost prohibitive now that the entire circuit is contained on a single substrate. Providing a separate substrate for the power stage would require expensive hand interconnection. The only acceptable porcelain on steel design (Z), is much too heavy.

Aluminum is probably, again, the best frame candidate for the advanced packaging design. A more accurate analysis will probably yield an improvement from 25% to 50% in thermal performance. This will make design (U) a viable thermal performer at very low weight.

3.4 Rating Populations

The low profile of the chip carriers allows the controllers to be mounted on both sides of a center frame. Two 5a, 2a, or 1/2A controllers, per side, can be placed on each frame by staggering the positions of the power FET's on an opposing side of the frame. (See Fig. 3-8). NOTE: Only one power FET is required for 5a, 2a and 1/2a controllers. The 10a controller is constrained by thermal considerations from being mounted back-to-back on the same frame. Table 3-3 lists the results of two 10a controllers mounted back-to-back on module designs S to Z. Each controller is assumed to use only 1/2 the frame thickness to conduct the heat to the rib. Design V and W might be capable of handling the increased heat load but the cost gain achieved by doubling the population would have to be compared to the cost penalty of using BeO substrates in design (V) and both BeO substrates and a copper frame in design (W) which also weighs twice as much as the aluminum frame designs. Also, effects on reliability, due to higher operating temperatures, would have to be determined.

3.5 Reliability

To calculate the predicted reliability of a 10 amp DC controller packaged on an ISEM-2A module, use will be made of the Reliability Prediction for the DC controller found in Appendix B. The analysis presented in that report is based upon failure rates given in MIL-HDBK-217B. This document has been superseded by MIL-HDBK-217C which, among other things, has reduced the failure rate of diodes by 70% and transistors

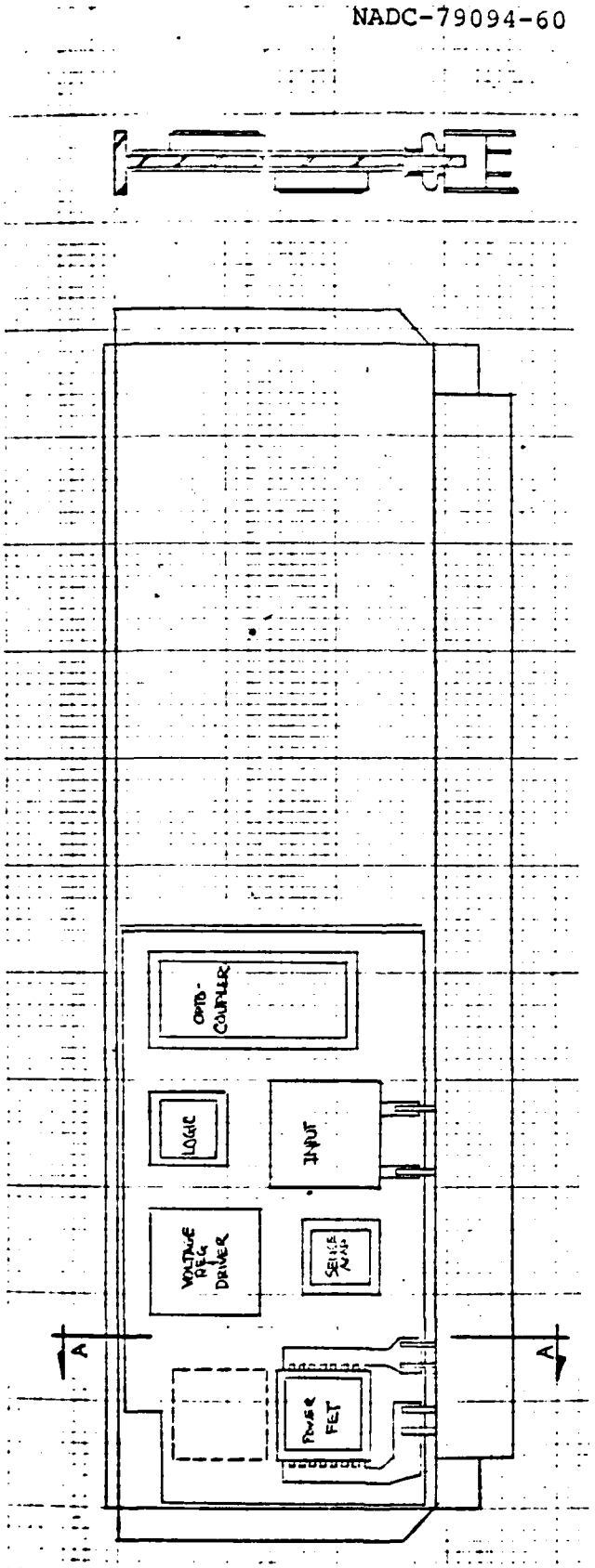


FIGURE 3-8. MOUNTING OF FOUR 5, 2 OR 1/2 AMP UNITS ON "T" FRAME

TABLE 3-3. Thermal Performance of Designs With Heat Sources on Opposite Sides of Frames

	T	U	V	W	X	Y	Z	S
$\theta_{P\ To\ T}$	1.47	1.00	.22	.17	.41	3.71	.57	1.50
$\theta_{L\ To\ T}$	7.46	7.46	3.7	2.6	7.03	8.4	8.0	6.99
$\theta_{RT(^{\cdot}C/W)}$	8.9	8.5	3.9	2.8	8.0	12.1	8.57	8.49
T(°C)	134°C	128°C	59°C	42°C	120°C	182°C	129°C	127°C
@T_{RIB} = 70°C $\Delta T_{Component}$ (θ C)	234°C	228°C	159°C	142°C	220°C	282°C	229°C	227°C

$\theta_{CONTACT}$ = 2.0 °C/W $T_{CONTACT}$ = 30°C

W/IERC CLIP Imp.

by 40%. These factors will be used in computations of the predicted reliability of a controller using advanced packaging concepts for a 10 amp ISEM-2A module.

The calculated reliability of the ISEM-2A controller is made by factoring failure rates, determined in Appendix B, in accordance with elimination of parts and changes in part failure rates as mentioned previously. Referring to Table C of Appendix B, the total IC failure rate can be reduced from .5212 to .3619 $f/10^6$ hrs. by combining the 6 IC's into two MSI chip carriers. The transistor failure rate can be reduced from 0.3681 to 0.1105 $f/10^6$ hrs. because of parts reduction and lower part failure rate prescribed by MIL-HDBK-217C. The same reasons apply to diodes where the failure rate is reduced from 0.0582 to 0.0136. Adding these failure rates to the rates for opto-couplers and capacitors, results in

$$\sum N_C \lambda_C \pi_G = 0.6348 \text{ f/}10^6 \text{ hrs.}$$

Referring to page 3 of Appendix B, the reduction in number of screened resistors results in -

$$(N_N \lambda_R + \sum N_I \lambda_I + \lambda_s) \pi_F \pi_E = 0.2478 \text{ f/}10^6 \text{ hrs.}$$

Combining the above failure rates and applying factors

ISEM-2A λ_p = (0.6348 + 0.2478) x 1.16 =

1.0238 $f/10^6$ hrs.

ISEM-2A MTBF = $\frac{1}{\lambda_p}$ = 977,000 hours/failure

By comparison, using the new failure rates for semiconductors which are prescribed by MIL-HDBK-217C, and which were used in the above MTBF calculation, the reliability of the present 10A. DC controller developed under Contract No. N62269-77-C-0413 is calculated to be 740,000 hours per failure.

4.0 CONCLUSIONS

The solid state DC controller which was developed under Contract No. N62269-77-C-0413, can be packaged onto ISEM-2A modules, using the existing technology. However, only one controller per frame is possible and manufacture would be relatively expensive.

With circuit simplification brought about by using power FET devices and by employing LSI technology to compact segments of the control circuit module, populations can be increased four-fold. Using leadless chip carrier fabrication techniques will improve manufacturability and repairability markedly, as well as reducing cost. A conservative thermal analysis was used to rank the various frame designs. A design comprised of alumina substrate soldered to an extruded aluminum frame is the best design choice, due to its adequate thermal performance, coupled with its low weight and cost and ease of manufacturing.

By using advanced packaging concepts and circuit simplifications as described in Section 3, the reliability of a 10A DC controller on an ISEM-2A frame will be increased by a factor of 32% as compared to the present DC controller.

The following populations of the four DC controller ratings can be mounted on ISEM-2A single-sided "L" frames and double-sided "T" frames:

Controller Rating	ISEM-2A "L" Frame	ISEM-2A "T" Frame
10 Amp.	2	--
5 Amp.	2	4
2 Amp.	2	4
1/2 Amp.	2	4

All of these configurations of DC power controllers, which meet the electrical requirements of specification NADC-30-TS-7602, dated 27 April 1976, are considered to be within the physical and thermal constraints of modular avionics packaging (MAP) concepts.

APPENDIX A

Data Sheet for High Power MOSFET Type IRF-150, Manufactured by International Rectifier.

Data Sheet No. PD-9.305A
Revised June 1979

INTERNATIONAL RECTIFIER

100 Volt, 0.055 Ohm HEXFET™

The HEXFET™ technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

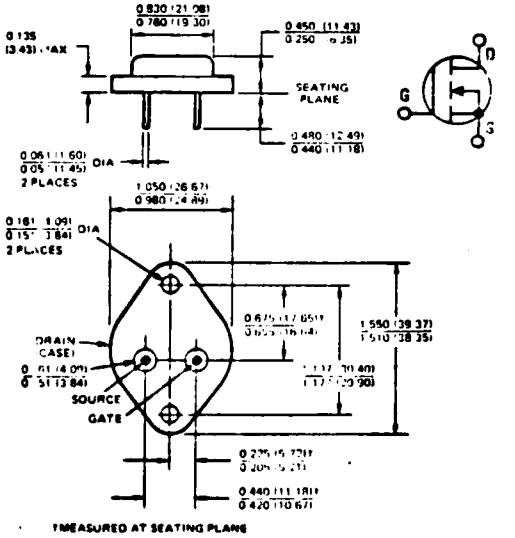
They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

FEATURES:

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

PRODUCT SUMMARY

PART NUMBER	V_{DS}	$R_{D(on)}$	I_D
IRF150	100V	0.055Ω	28A
IRF151	60V	0.055Ω	28A
IRF152	100V	0.08Ω	24A
IRF153	60V	0.08Ω	24A



H-1 Case (Modified TO 204AA(TO3))
Dimensions in Inches and (Millimeters)

IRF150, IRF151, IRF152, IRF153 DEVICES
MOSFET TRANSISTORS – DATA SHEET NO. PD-9.305A
REVISED JUNE 1979

Absolute Maximum Ratings

Parameter		IRF150	IRF151	IRF152	IRF153	Units
V_{DS}	Drain – Source Voltage	100	60	100	60	V
V_{DGR}	Drain – Gate Voltage ($R = 1\ M\Omega$)	100	60	100	60	V
I_D	Continuous Drain Current	28		24		A
I_{DM}	Pulsed Drain Current	70		60		A
V_{GS}	Gate – Source Voltage	±20				V
P_D	Max. Power Dissipation	150 (See Fig. 11)				W
	Linear Derating Factor	1.2 (See Fig. 11)				W/deg C
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH				A
		70		60		
T_J T_{stg}	Operating and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10 sec)				°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	IRF150 IRF152	100			V	V_{GS} = 0
		IRF151 IRF153	60			V	I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	1.		3	V	$V_{DS} = V_{GS}$, I_D = 1 mA
I_{GSS}	Gate – Body Leakage	ALL			100	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL		0.1	1.0	mA	V_{DS} = Max. Rating, V_{GS} = 0
				0.2	4.0	mA	V_{DS} = Max. Rating, V_{GS} = 0, T_J = 125°C
$I_{D(on)}$	On-State Drain Current	IRF150 IRF151	28			A	V_{DS} = 25V, V_{GS} = 10V
		IRF152 IRF153	24			A	
$R_{DS(on)}$	Static Drain-Source On State Resistance	IRF150 IRF151		0.045	0.055	Ω	V_{GS} = 10V, I_D = 14A
		IRF152 IRF153		0.06	0.08	Ω	
g_{fs}	Forward Transconductance	ALL	6	10		S (℧)	V_{DS} = 25V, I_D = 14A
C_{iss}	Input Capacitance	ALL		3000	4000	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz (See Fig. 10)
C_{oss}	Output Capacitance	ALL		1900	1500	pF	
C_{rss}	Reverse Transfer Capacitance	ALL		350	500	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL		40	60	ns	I_D = 14A, E_1 = 0.5 BV_{DSS} (See Figs. 12 and 13) T_J = 125°C (MOSFET Switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL		150	200	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL		200	300	ns	
t_f	Fall Time	ALL		150	200	ns	

Thermal Characteristics

$R_{\theta JC}$	Maximum Thermal Resistance Junction-to-Case	ALL	0.83	deg C/W	

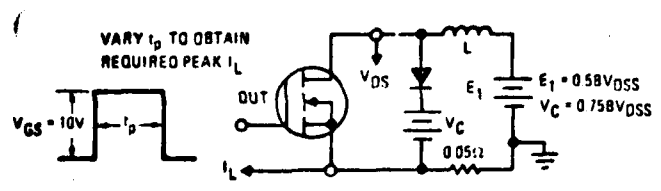


Fig. 1 – Clamped Inductive Test Circuit

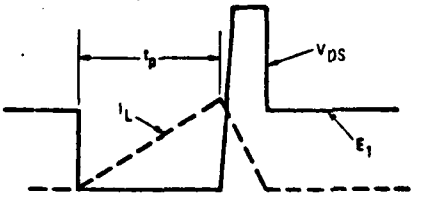


Fig. 2 – Clamped Inductive Waveforms

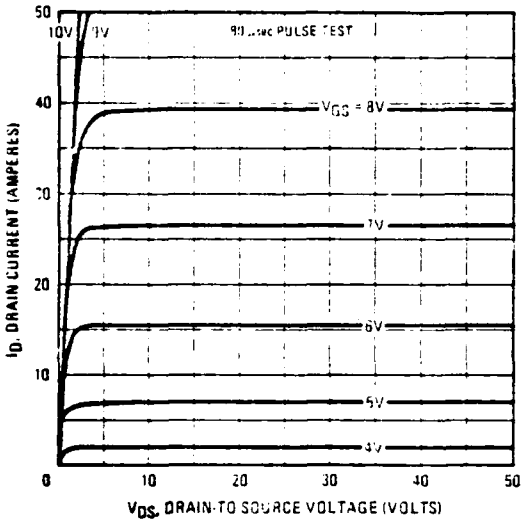


Fig. 3 – Output Characteristics

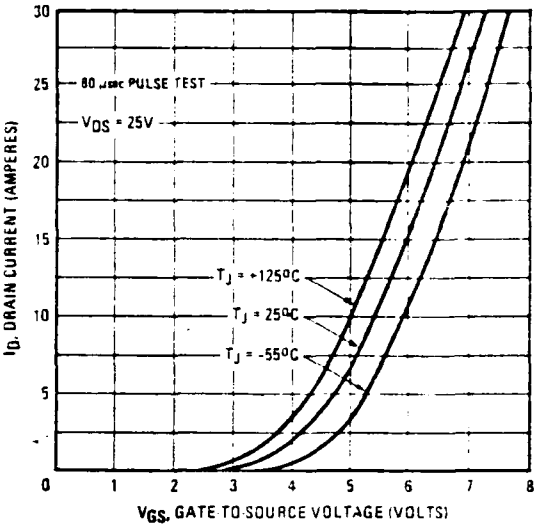


Fig. 4 – Transfer Characteristics

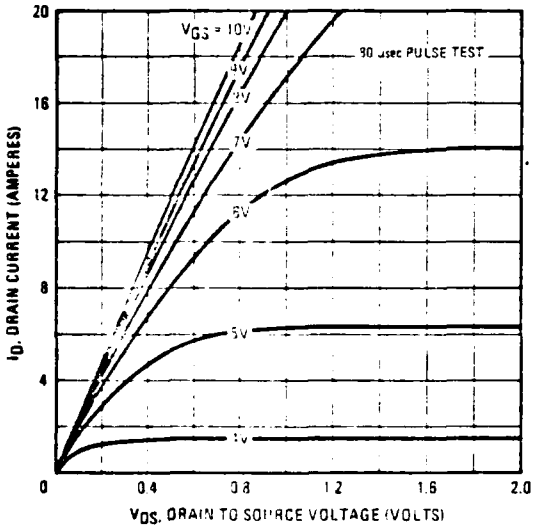


Fig. 5 – Saturation Characteristics (IRF150, IRF151)

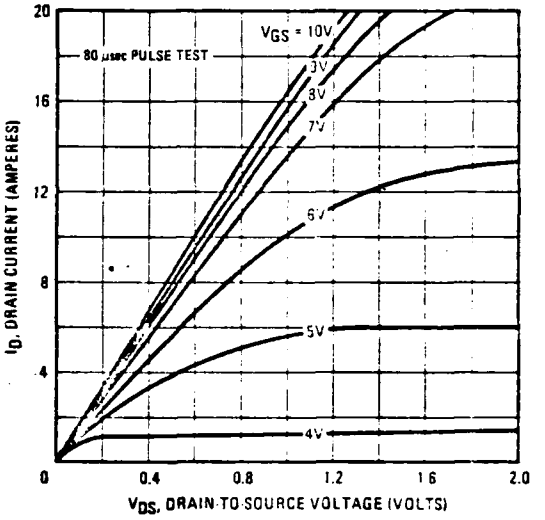


Fig. 6 – Saturation Characteristics (IRF152, IRF153)

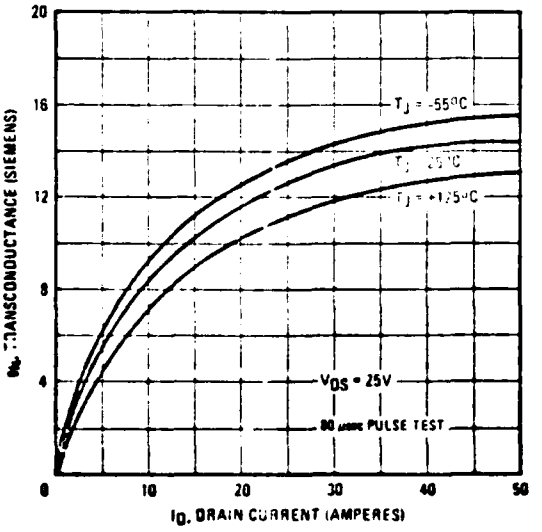


Fig. 7 – Transconductance Vs. Drain Current

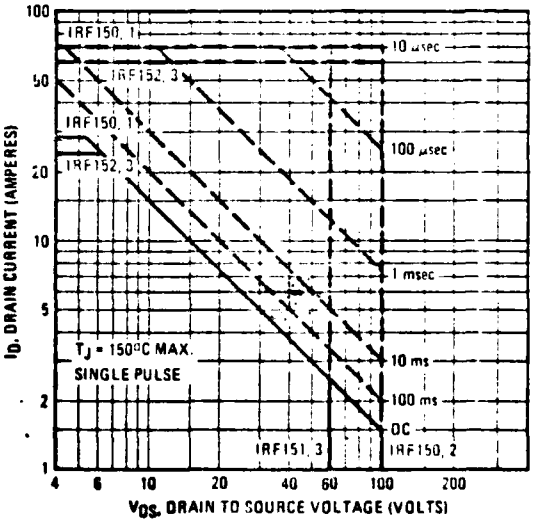


Fig. 8 – Maximum Safe Operating Area

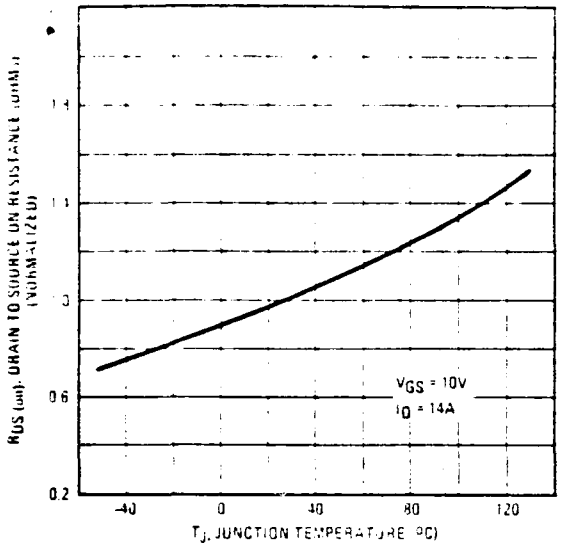


Fig. 9 – Normalized On-Resistance Vs. Temperature

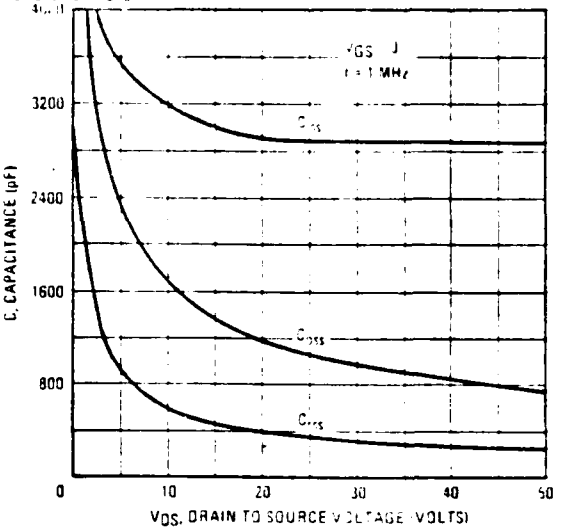


Fig. 10 – Capacitance Vs. Drain-to-Source Voltage

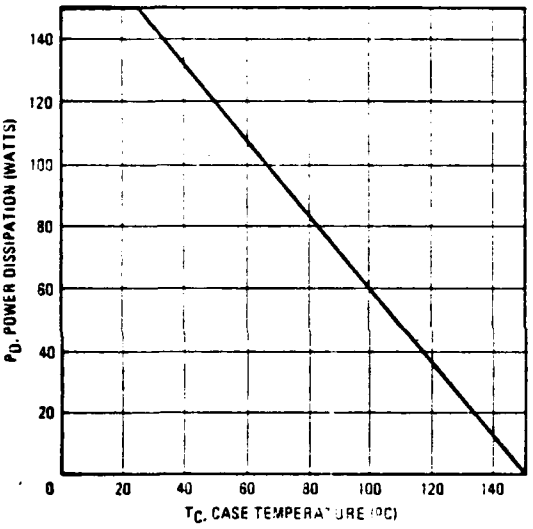


Fig. 11 – Power Vs. Temperature Derating

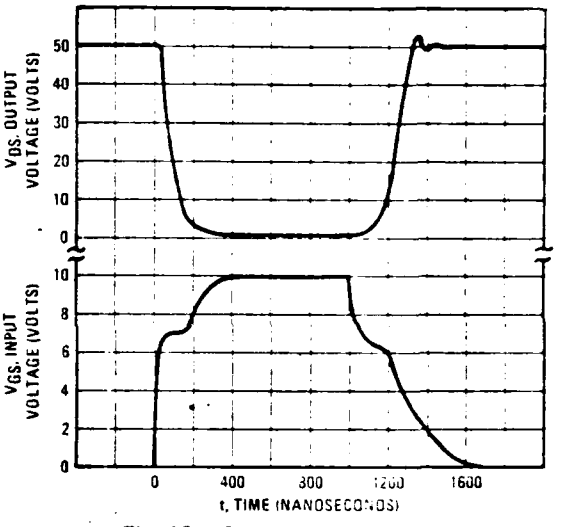


Fig. 12 – Switching Waveforms

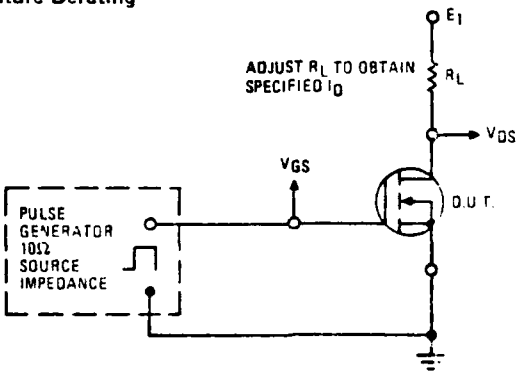


Fig. 13 – Switching Time Test Circuit

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APPENDIX B

RELIABILITY PREDICTION

FOR

POWER CONTROLLER - DC, LOAD SWITCHING

23 JUNE 1978

CONTRACT NO. N62269-77-C-0413

PREPARED FOR:

NAVAL AIR DEVELOPMENT CENTER
WARMINSTER, PA. 18974

Prepared by:

RCA
Government Communications Systems
Camden, N. J. 08102

FOREWORD

This Reliability Prediction is submitted as required under Contract N62269-77-C-0413. It is identified as Item A003 in the Contract Data Requirements List (DD 1423) and is part of Contract Line Item 0005AA. The content and format of this plan comply with the requirements of Data Item Description DI-R-2117 and Work Statement Paragraph 9.3.

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LIST OF TABLES

D.C. Controller Reliability Analysis and MTBF Prediction

This analysis fulfills the requirements of CDRL Sequence No. A003, Reliability Prediction Report. It has been conducted in accordance with Task R2, Reliability Analysis and Prediction, of the D.C. Power Controller Reliability Program Plan, 15 October 1977.

1. Design Basis for Prediction

A third MTBF prediction has been performed for the D.C. Controller; it updates the second MTBF prediction of 23 March 1978. This prediction is based on the D.C. Controller design as of 15 June 1978.

2. Reliability Model and Prediction Method

The D.C. Controller is a microelectronics hybrid device. The new hybrid failure rate prediction model and procedure of Notice 2 to MIL-HDBK-217B, Reliability Prediction of Electronic Equipment, Section 2.1.7, was employed. This prediction method requires identification of individual electronic parts and substrates, and individual electrical stress data for each part. Thermal stress is caused by the hybrid package temperature and part power dissipation.

3. Design Data Sources

The failure rate (F.R.) and MTBF prediction is based on design information updating which has occurred after 10 March 1978. The identification of parts came from design engineering. Parts stress data were obtained from analysis of the updated circuit schematic drawings, May 1978. Additional data on parts and data on substrates were gotten from the circuit and hybrid designers. Integrated circuit and discreet semiconductor information was obtained from manufacturers' handbooks. The substrate areas were taken from the logic/amplifier and power deck (substrates) drawings included in the second design review data package.

4. Prediction Analysis

4.1 Data Base

The following items summarize the data base for the F.R. prediction:

		Dimensions in Inches	Quantity of Film Resistors N_R
(1)	Substrates:		
	(a) Thick film, Power	1.40 x 0.80	16
	(b) Thick film, Logic and Amplifier (2 layers)	1.10 x 1.30	44

(2) Active, Capacitor, and Packaged Parts or Chips:

There are 47 discretes as detailed in the Failure Rate Summary, Table C. The diodes and transistors are JAN or equivalent quality.

(3) Package:

Cold-rolled steel platform base and top hat soldered lid (bright tin plated) with insulated connection pins extending through the base: perimeter 6.0 inches, height 0.75 inches.

(4) Operating Environment:

Airborne, Uninhabited

(5) Screening Class (Quality Level) for D.C. Controller:
Class B (This is the expected screening level for quantity production.)

(6) Hybrid Package Mounting Base Temperature: 25°C
This is the near-center temperature between the extremes of the operating range: -54°C to +120°C.

4.2 Prediction Model and Calculations (per MIL-HDBK-217B, Notice 2, Section 2.1.7)

The hybrid failure-rate prediction math model is:

$$\lambda_p = \left[\Sigma N_C \lambda_C \pi_G + \left(N_R \lambda_R + \Sigma N_I \lambda_I + \lambda_S\right) \pi_F \pi_E\right] \pi_Q \pi_D$$

(failures/10^6 hr.)

Where:

$\Sigma N_C \lambda_C \pi_G$	is the sum of the adjusted failure rates for the active components and capacitors in the hybrid from section 2.1.7.1. N_C is the number of each particular component λ_C is the component failure rate π_G is the die correction factor Table 2.1.7-1
$N_R \lambda_R$	is the number of (N_R) and failure rate contribution (λ_R) of the chip or substrate resistors (section 2.1.7.2)
$\Sigma N_I \lambda_I$	is the sum of the failure rate contributions of the inter-connections (λ_I) from section 2.1.7.3
λ_S	is the failure rate contribution of the hybrid package. (Table 2.1.7-4)
π_E	is the Environmental Factor for the film resistors, interconnections and package from Table 2.1.7-5
π_Q	is the quality factor from Table 2.1.7-6
π_D	is the density factor from Table 2.1.7-7
π_F	is the circuit function factor = 1.0 for digital hybrids = 1.25 for linear or linear-digital combinations

Note: References to Table 2.1.7-X and section 2.1.7.Y are from MIL-HDBK-217B. Tables A through H are in this report.

For the D.C. Controller hybrid:

π_Q = 1.0 From Table 2.1.7-6 (Procured to MIL-M-38510, Appendix G and MIL-STD-883, Method 5004, Class B)

π_D = 1.16 (from Table 2.1.7-7) using the Density calculated as follows:

Density = $\frac{\text{No. of Interconnections}}{A_S + .10}$ where A_S = substrate area (sq. inches)

Each of two upper substrates: 1.1. in. x 1.3 in = 1.43 in.
lower substrate: 0.8. in. x 1.4. in. = 1.12 in.

Total A_S = 2 x 1.43 + 1.12 = 3.98 in.^{2}

$$\text{Density} = \frac{166 \text{ interconn's}}{(3.98 + 1.0)\ \text{in}^2} = \frac{166}{4.08} = 40.69\ \frac{\text{interconnections}}{\text{in}^2}$$

π_F = 1.25 (ea. of the 3 substrate is a linear-digital combination)

π_E = 3.0 (from Table 2.1.7-5)

λ_S = pkg. F.R. = .0339 f/10^6 hrs. (from Table 2.1.7-4) for Seal perimeter = 6.0 inches and T = pkg. temp. = 25°C

For the 10 ampere controller (using Tables A and B):

$$(N_N\lambda_R + \Sigma N_I\lambda_I + \lambda_S)\pi_F\pi_E = (.0060 + .0289 + .0339)(1.25)(3.0) = .2580 \text{ f/}10^6\text{hrs}$$

For the 10 amp. controller:

$\Sigma N_C\lambda_C\pi_G$ = 1.0962 f/10^6 hrs. (from Table C)

Using the hybrid model equation and substituting the calculated F.R.'s and π factors:

10 amp. Hybrid λ_p=[1.0962 + 0.2580] x 1.0 x 1.16 = 1.5709 f/10^6 hrs.

$$\text{10 amp. Hybrid MTBF} = \frac{1}{\text{Hybrid } \lambda_p} = \frac{1}{1.57 \times 10^{-6} \text{ failures/hour}} =$$

635,000 hours/failure

For the 5 ampere controller, two RCA 57654 transistors, two 2N6318, and 2 substrate film resistors are not needed so that the corresponding failure rates are substracted from the 10 ampere controller failure rate. The resulting failure rate is 1.4316 failures per 10^6 hours. This corresponds to an MTBF of 700,000 hours.

For the 2 ampere and 1/2 ampere controllers an additional RCA 67654 transistor, a 2N6318, and a resistor are not needed (compared to the 5 ampere controller). The resulting failure rate is 1.3619 failures per 10^6 hours. The MTBF is 735,000 hours.

The MTBF's calculated above include the effect on MTBF of the two optocouplers used for trip and fault reporting. Should either of these two devices fail, the controller will still perform its major functions of load on-off switching and tripping open upon overload. If the two optocouplers are removed from the calculations, the following slightly-improved MTBF's result.

10 ampere controller:	640,000 hours
5 ampere controller:	705,000 hours
2 or 1/2 ampere controller:	740,000 hours

4.3 MTBF Objective

The MTBF objective is 1.34×10^6 hours per failure. It appears that this objective is too high for the D.C. Controller, operating in the severe airborne uninhabited environment, because it has significant functional capability and complexity, with the consequent hardware complexity. Six IC's, 20 transistors, 9 diodes, 3 optocouplers, 9 capacitors, and 60 resistors are needed to provide the specified functions. Even with the new hybrid prediction method of Notice 2 to MIL-HDBK-217B, and the low stresses seen by the parts, the sum of predicted failure rates of the parts produces an MTBF about two-to-one lower than the MTBF objective.

TABLE A

Hybrid Resistor Failure Rate Calculation
Either chip or substrate R's

(from 2.1.7.2 of MIL-HDBK-217B, Notice 2, 17 Mar. 1978)

N_R = no. of (chip or) substrate R's = 60

λ_R = F.R. of (chip or) substrate R's = .00010 f/10^6 hr (for T≤50°C) from Table 2.1.7-2 where T is the hybrid pkg. temp.

$\lambda_{\text{hybrid R's}} = N_R\lambda_R$ = 60 x .00010 f/10^6 hrs = .0060 f/10^6 hrs.

TABLE B

Hybrid Interconnection Failure Rate Calculation

	Item Qty.	$N_{I/ITEM}$	QN_I
Ea. IC chip bonding pad	78	1	78
U7 8 bonding pads U1 14 bonding pads U2 14 bonding pads U3 14 bonding pads U5 14 bonding pads U6 14 bonding pads			
Total 78 bonding pads			
Ea. Transistor	20	2	40
Ea. Diode	8	1	8
Ea. Capacitor	9	2	18
Ea. External Lead	20	1	20
Ea. External Diode	1	2	2

No of Interconnections = ΣN_I = 166

at 25°C package temp

$\lambda_{I_1} = \lambda_{I_2}$ = .000174 f/10^6 hrs. (from Table 2.1.7-3)

hence: $\Sigma N_I \lambda_I$ = 166 x .000174 f/10^6 hrs. = .0289 f/10^6 hrs.

TABLE C

Active Parts and Capacitors Failure Rate Summary
($\Sigma N_C \lambda_C \pi_G$ = sum of adjusted λ's for active components and capacitors)

	$\lambda_T \pi_G$	Reference
6 IC's	.5212 f/10^6 hrs.	TABLE D
20 Transisors	.3681 "	TABLE E
9 Diodes	.0582 "	TABLE F
3 Optocouplers	.0234 "	TABLE G
9 Capacitors	.1254 "	TABLE H
$\Sigma N_C \lambda_C \pi_G$ =	1.0963 "	

TABLE D

INTEGRATED CIRCUITS & FAILURE RATE CALCULATION (T_A = 25°C)

3 CMOS Digital IC's:

	π_L	π_P	Gates	T_J	π_{T2}	C_1	C_2	π_Q	π_E
CD4070B	1.0	1.0	4	30°C	.155	.0033	.0064	2	6
CD4001B	1.0	1.0	4	30°C	.155	.0033	.0064	2	6
CD4011B	1.0	1.0	4	30°C	.155	.0033	.0064	2	6

CMOS IC: $\lambda_p = \pi_L \pi_Q (C_1 \pi_{T2} + C_2 \pi_E) \pi_p$ f/10^6 hrs.

$= 1 \times 2 (.0033 \times .155 + .0064 \times 6) \times 1$
$= 2(.00051 + .0384) \times 1$
$= .0778$ f/10^6 hrs for ea. CMOS IC

3 Linear Bipolar IC's:

	π_L	π_P	XSTRS	T_J	π_{T2}	C_1	C_2	π_Q	π_E
CA 124	1.0	1.0	52	35°C	.24	.011	.023	2	6
CA 139	1.0	1.0	32	35°C	.24	.0079	.017	2	6
LM 723	1.0	1.0	16	35°C	.24	.0046	.012	2	6

Linear IC: $\lambda_p = \pi_L \pi_Q (C_1 \pi_{T2} + C_2 \pi_E)$

CA 124: $\lambda_p = 1 \times 2(.011 \times .24 + .023 \times 6) = .2813$ f/10^6 hrs.

CA 139: $\lambda_p = 1 \times 2(.0079 \times .24 + .017 \times 6) = .2078$ f/10^6 hrs.

LM 123: $\lambda_p = 1 \times 2(.0046 \times .24 + .012 \times 6) = .1462$ f/10^6 hrs.

λ_T for 6 IC's:
.0778 f/10^6 hrs.
.0778 f/10^6 hrs.
.0778 f/10^6 hrs.
.2813 f/10^6 hrs.
.2078 f/10^6 hrs.
.1462 f/10^6 hrs.
λ_T = .8687 f/10^6 hrs.
x .6 ($=\pi_G$) adjustment factor for dies
Adjusted F.R. = $\pi_G \lambda_T$ = .52122 f/10^6 hrs.

TABLE E

Transistor Failure Rate Calculation

$\pi_G = .4$ $\quad \pi_E \pi_Q = 8$ $\quad \pi_E = 40(A_u)$, $\pi_Q = .2$(JANTXV), $T_A = 25°C$

Part type (GRP I)	GRP I	QTY	λ_b	Polarity	S	π_A	π_R	π_{S2}	π_C	Ratings P(W)	Ratings V_{CEO}
RCA 67654(TA8660)		4	.0046	NPN	<.1	.7	5.0	.48	1.0	175	80
2N6318 MOT		4	.0065	PNP	<.1	.7	5.0	.48	1.0	90	80
2N6316 MOT		2	.0046	NPN	.1	1.5	5.0	.30	1.0	90	80
2N5339 MOT		1	.0046	NPN	.1	.7	2.0	.36	1.0	6.0	100
2N3019		2	.0046	NPN	.1	1@.7 1@1.5	1.5	.30	1.0	>1to5	80
2N5550 MOT		4	.0046 .0075	NPN	.1 .4	3@ .7 1@1.5	1.0	.30	1.0	1.0	140
2N2484		2	.0046	NPN	.1	1@.7 1@1.5	1.5	.30	1.0	1.2	60
2N3251		1	.0065	PNP	.1	.7	1.5	.30	1.0	1.2	40

$N\lambda_p = \frac{N}{4} \times \frac{\lambda_b}{.0046} \times \frac{\pi_A}{.7} \times \frac{\pi_R}{5.0} \times \frac{\pi_{S2}}{.48} \times \frac{\pi_E \pi_Q \pi_C}{8}$ $\quad = 6.72 \times .0111 = .074592$ $\quad \frac{N\lambda_b \pi_A \pi_R \pi_{S2}}{}$

(4) TA 8660		
(4) 2N6318	4 x .0065 x .7 x 5.0 x .48	
(2) 2N6316	2 x .0046 x 1.5 x5.0 x .30	.020700
2N5339	1 x .0046 x .7 x 2.0 x .36	.002318
(1) 2N3019, (1) 2N2484	2 x .0046 x .7 x 1.5 x .30	= 2.2 x .00414=.009108
(1) 2N3019, (1) 2N2484	2 x .0046 x1.5 x 1.5 x .30	
2N5550	1 x .0075 x1.5 x 1.0 x .30	.003375
2N3251	1 x .0065 x .7 x 1.5 x .30	.002048
(3) 2N5550	3 x .0046 x .7 x 1.0 x .30	.002893
λ_T for 20 XSTRS = $\Sigma N_i \lambda_{pi}$ = .9203 f/10^6 hrs. =	8 x	.115039

$\lambda_T \pi_G$ = .9203 x .4 = .3681 f/10^6 hrs. = adjusted F.R.

TABLE F

Diode Failure Rate Calculation

$\pi_G = .2$

$T_C = 25°C$

All JAN TXV, $\pi_Q = .5$, $\pi_E = 4.0$, $\pi_C = 1$

$\lambda_p = \lambda_b(\pi_E\pi_A\pi_Q\pi_R\pi_{S2}\pi_C)$

Part No.	Type	Qty	S	Group IV λ_B	π_A	π_R	π_{S2}	$\pi_E\pi_Q\pi_C$	Ratings I(A)	(PIV)
1N 4148	SW'G	3	.1	.0009	0.6	1.0	0.7	20	.2	100
1N 4148	SW'G	1	.1	.0009	1.0	1.0	0.7	20	.2	100
1N 4002	SW'G	1	.1	.0009	0.6	1.0	0.7	20	1.0	120

Group V $\lambda_p = \lambda_b(\pi_E\pi_A\pi_Q)$

Part No.	Type	Qty.	S	λ_b	π_A	$\pi_E\pi_Q$	P(W)
1N 747	Zener	1	.1	.0031	1.0	20	.4
MZ243B1♦	Zener	1	.1	.0031	1.0	20	
1N3040B	Zener	2	.1	.0031	1.0	20	1.0

	N	$N\lambda_p$ / λ_b	π_A	π_R	π_{S2}	$\pi_E\pi_Q$	π_C	$N\lambda_b\pi_A\pi_R\pi_{S2}$
(3) 1N4148, (1) 1N4002	4	.0009	0.6	1.0	0.7	20	1.0	.001512
(1) 1N4148	1	.0009	1.0	1.0	0.7	20	1.0	.000630
(1) 1N747	1	.0031	1.0			20		.012400
(1) MZ43B1♦	1	.0031	1.0			20		.014542
(2) 1N3040B	2	.0031	1.0			20		

20x

λ_T for 9 Diodes = $\Sigma N_i\lambda_{pi}$ = .2908 = 20 x .014542 f/10^6 hrs.

Adj. F.R. = $\lambda_T\pi_G$(diodes) = .29084 x .2 = .058168 = .0582 f/10^6 hrs.

TABLE G

Optocoupler Failure Rate Calculation

$\lambda_p = \lambda_b \pi_C \pi_E \pi_Q$ $\quad \pi_G = 1.0$ (packaged in metal cans)

$\pi_E = 6, \quad \pi_Q = 1$

Part No.	Qty(N)	S	λ_b	π_C	$\pi_E\pi_Q$	$N\lambda_p = N\lambda_b\pi_C\pi_E\pi_Q$
OPI 1991(OPI 140)	2	.1	.0006	1.5	6	0.0108 f/10^6 hrs.
OPI 1991(OPI 140)	1	.3	.0014	1.5	6	0.0126 f/10^6 hrs.
Adjusted F.R. = $\pi_G\lambda_T = \Sigma N_i\lambda_{pi}$ =						0.0234 f/10^6 hrs.

TABLE H

Capacitor Chip Failure Rate Calculation

$T_A = 25°C$, $\pi_G = 0.8$

H-1 Ceramic 125°C Rating $\lambda_p = \lambda_b(\pi_E\pi_Q)$ π_E=10, π_Q=1 (MIL-C-39014, level M)

λ_b on Table 2.6.4-4 (125°C Rating)

Part Type	Rated Voltage	Qty	S	λ_b	$\pi_E\pi_Q$	
CKR06 100,000pf	100	2	.1	.0019	10	$N\lambda_p = N\lambda_b\pi_E\pi_Q$
CKR05 10,000pf	100	2	.1	.0019	10	$N\lambda_p = 8 \times .0190 = .1520$ f/10⁶ hrs.
CKR05 1,000pf	200	4	.1	.0019	10	

H-2 Tantalum CSR $\lambda_p = \lambda_b\pi_E\pi_{SR}\pi_Q$ failures/10^6 hrs.

MIL-C-39003/1
1.0 µf, 50 Vdc $\lambda_p = .0046 \times 15 \times .07 \times 1.0$ f/10^6 hrs.
Qty = 1 = N

$N\lambda = N\lambda_p = .00483$ f/10^6 hrs.

π factors:
T_A=25°C, π_G=0.8
π_E=15, π_Q=1, π_{SR}=.07
S=.25 since applied voltage is 12.5 Vdc

$\lambda_T = \Sigma N_i\lambda_{pi} = .1520 + .00483 = .1568$ f/10^6 hrs.

Adjusted F.R. = $\pi_G\lambda_T = 0.8 \times .1568 = .12544$ f/10^6 hrs.